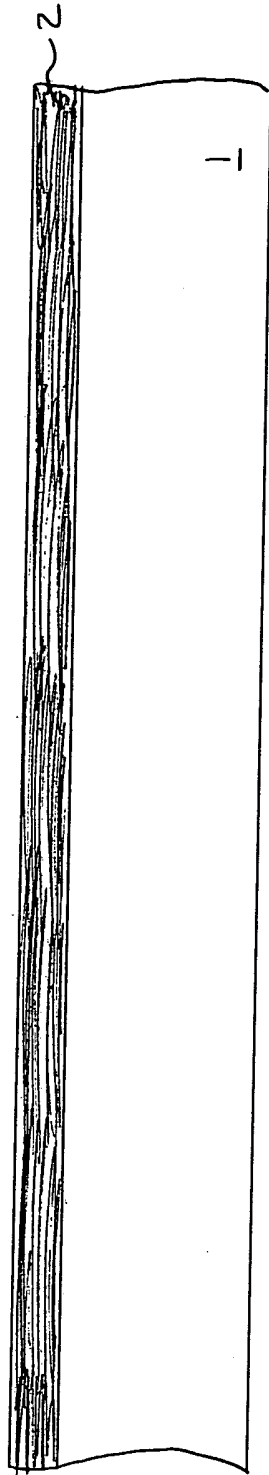


FIG. 1

FIG. 2



CONFIDENTIAL

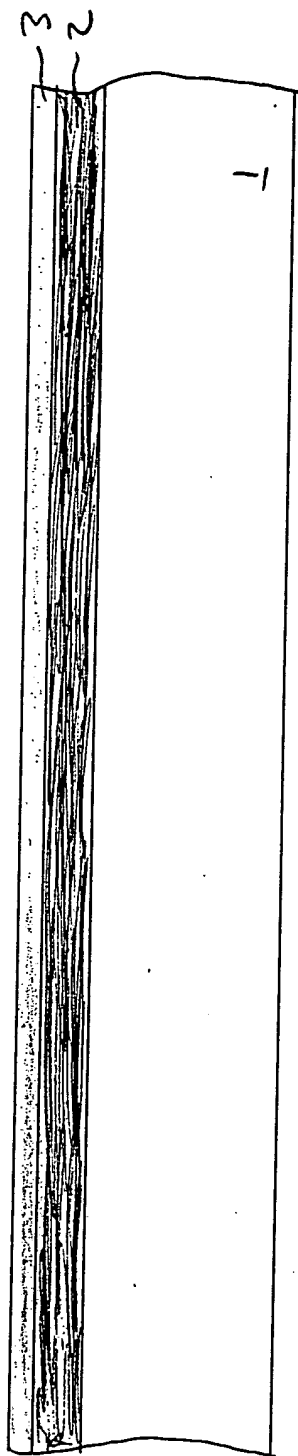


FIG. 3

FIG. 4A is a perspective view of a first embodiment of a device 100. The device 100 includes a main body 1 and a first end 4. The first end 4 is a rectangular block with a textured surface, which is attached to the main body 1. The main body 1 is a long, narrow, rectangular block with a smooth surface. The first end 4 is positioned at one end of the main body 1.

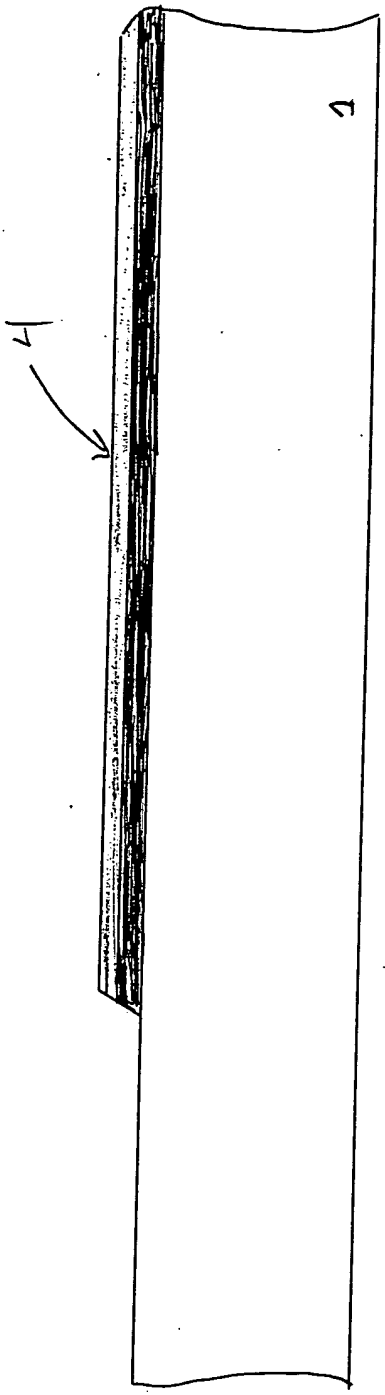


FIG. 4A

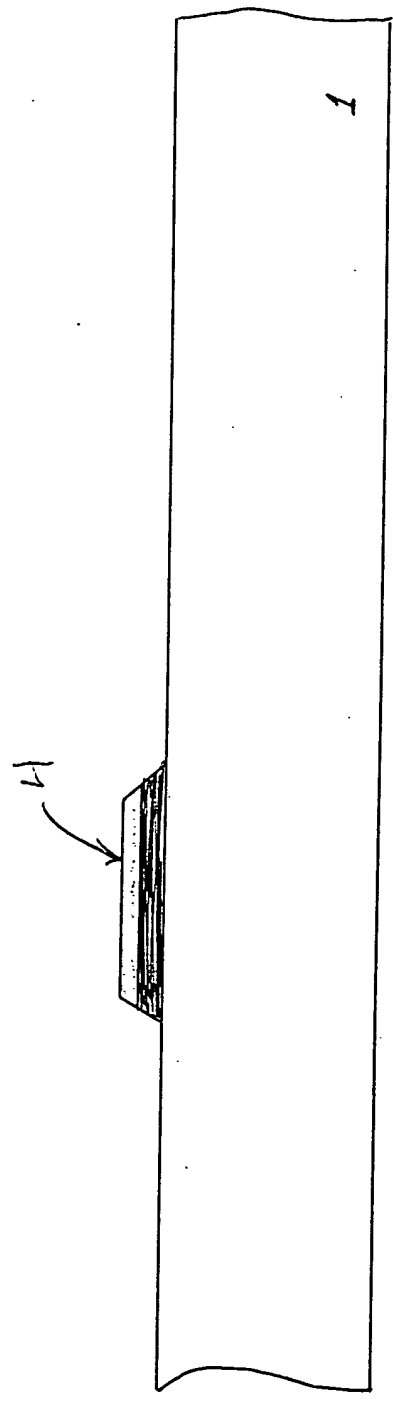


FIG. 4B

FIG. 5A

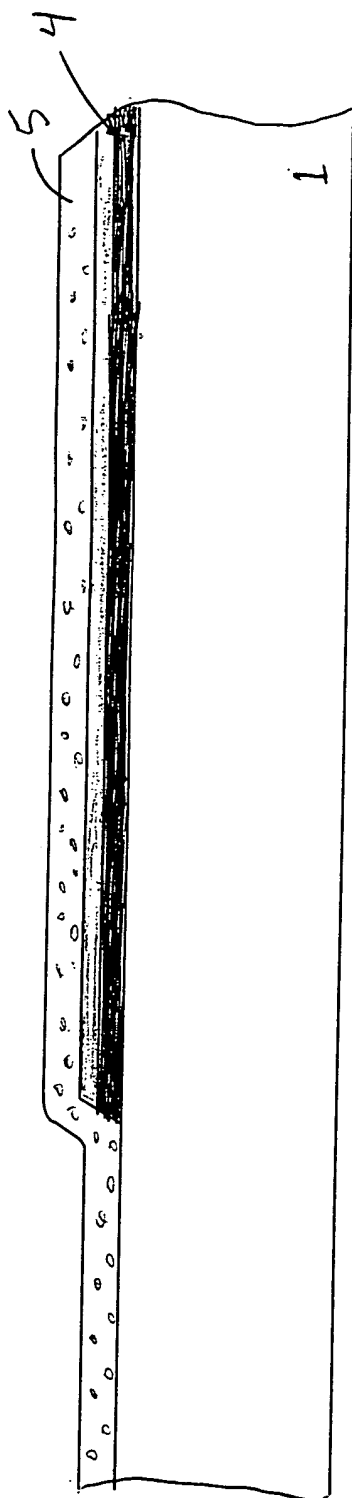


FIG. 5A

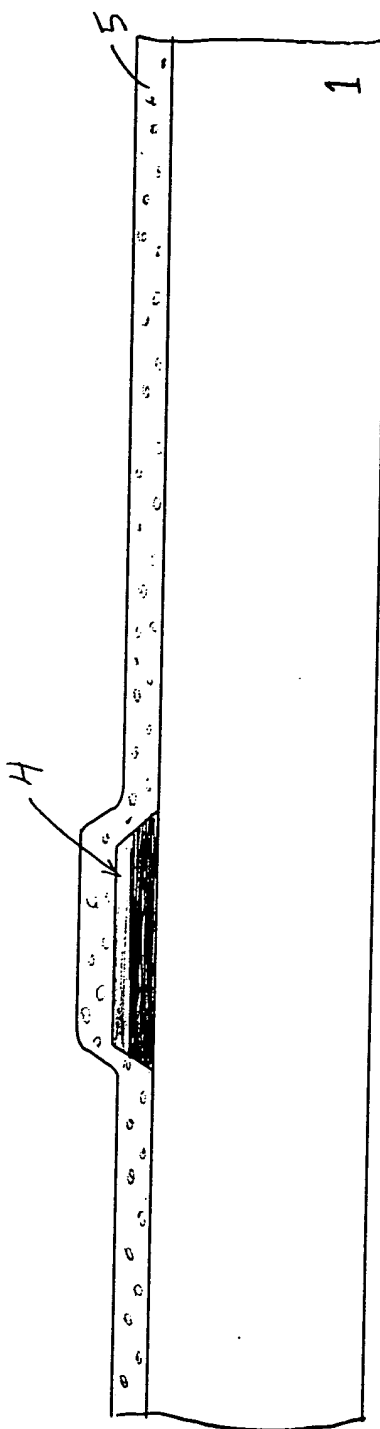


FIG. 5B

FIG. 6A is a perspective view of a first embodiment of a device 100, showing a main body 1, a top edge 5, and a bottom edge 6. A central longitudinal slot 4 is formed in the top edge 5, extending along the length of the device 100. The slot 4 is defined by a pair of parallel, slightly curved walls 4a and 4b, which are spaced apart to form a channel. The walls 4a and 4b are shown in cross-section, revealing a textured interior surface. The device 100 is shown in a perspective view, with the top edge 5 and bottom edge 6 clearly defined. The main body 1 is a rectangular structure with a slightly curved top edge 5 and a slightly curved bottom edge 6. The slot 4 is a longitudinal feature that runs the length of the device 100.

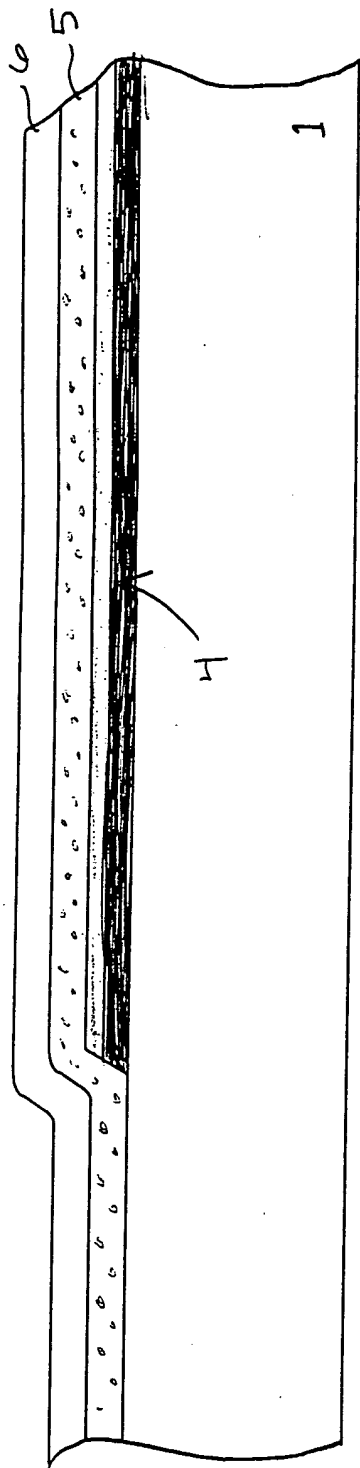


FIG. 6A

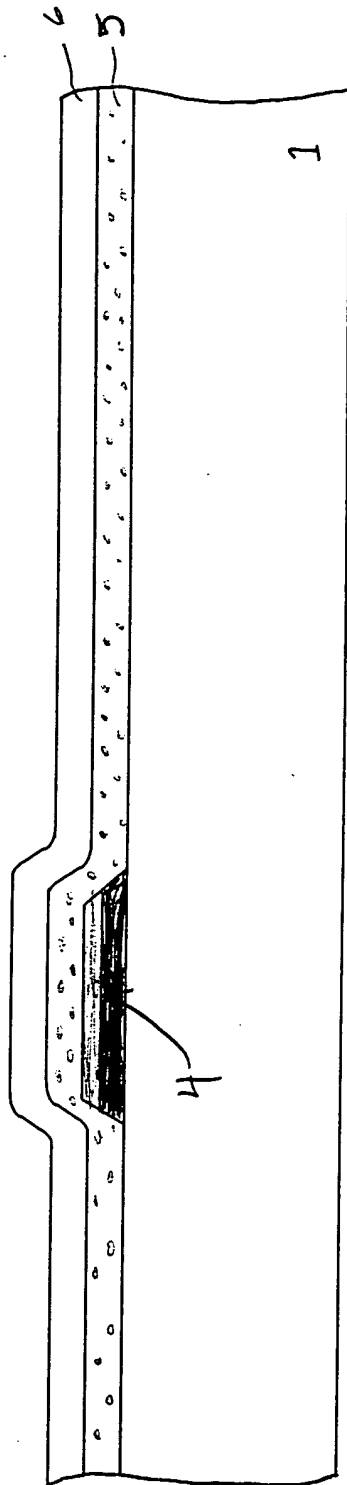


FIG. 6B

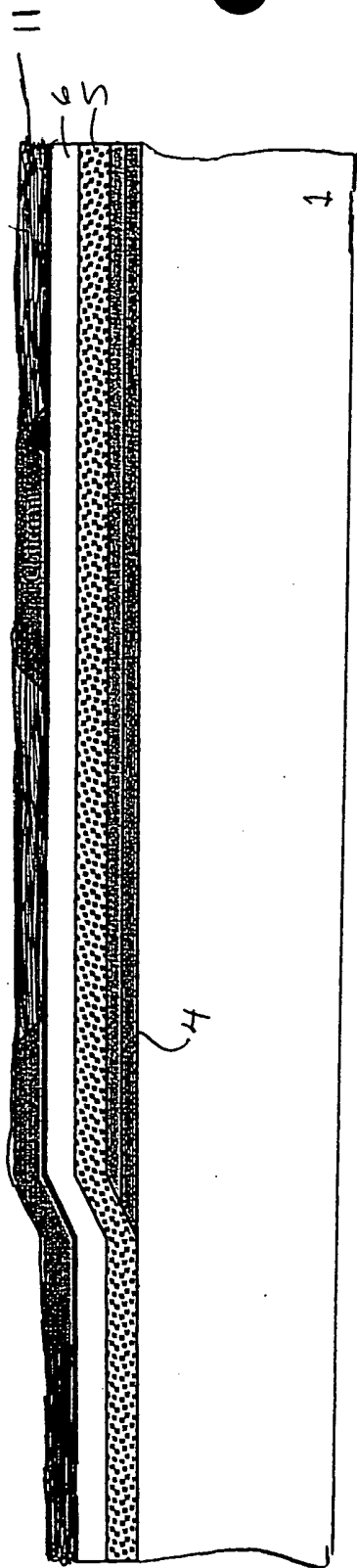


FIG. 7A

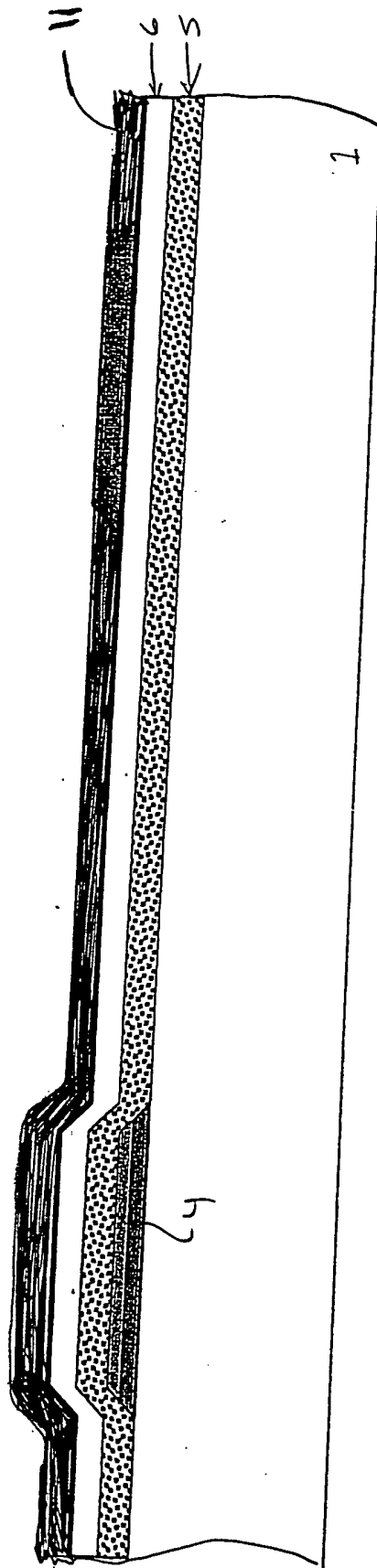


FIG. 7B

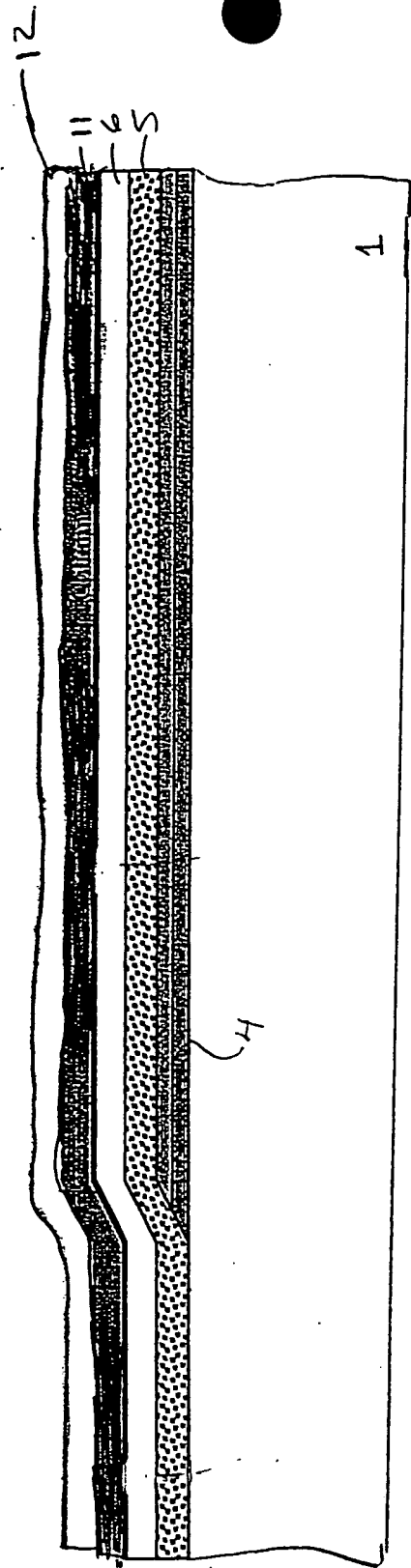


FIG. 8A

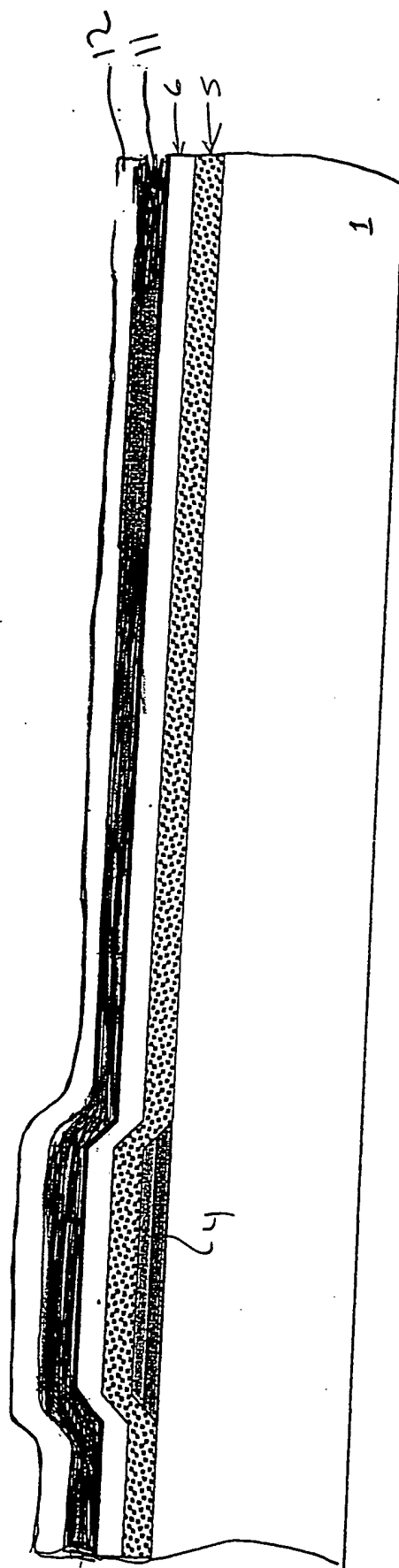


FIG. 8B

FIG. 9A

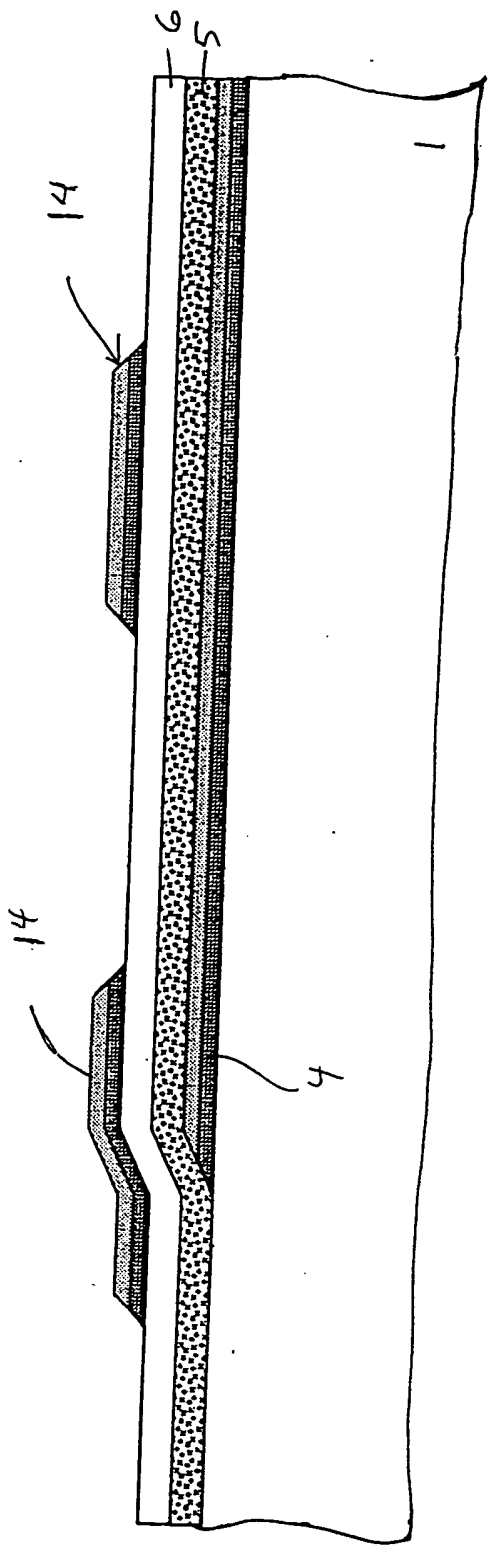


FIG. 9A

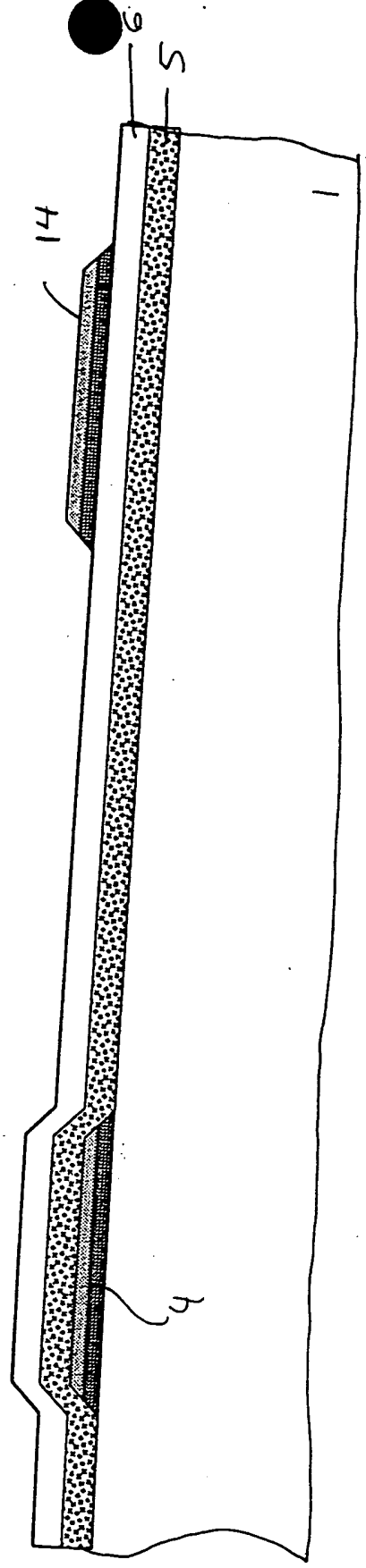


FIG. 9B

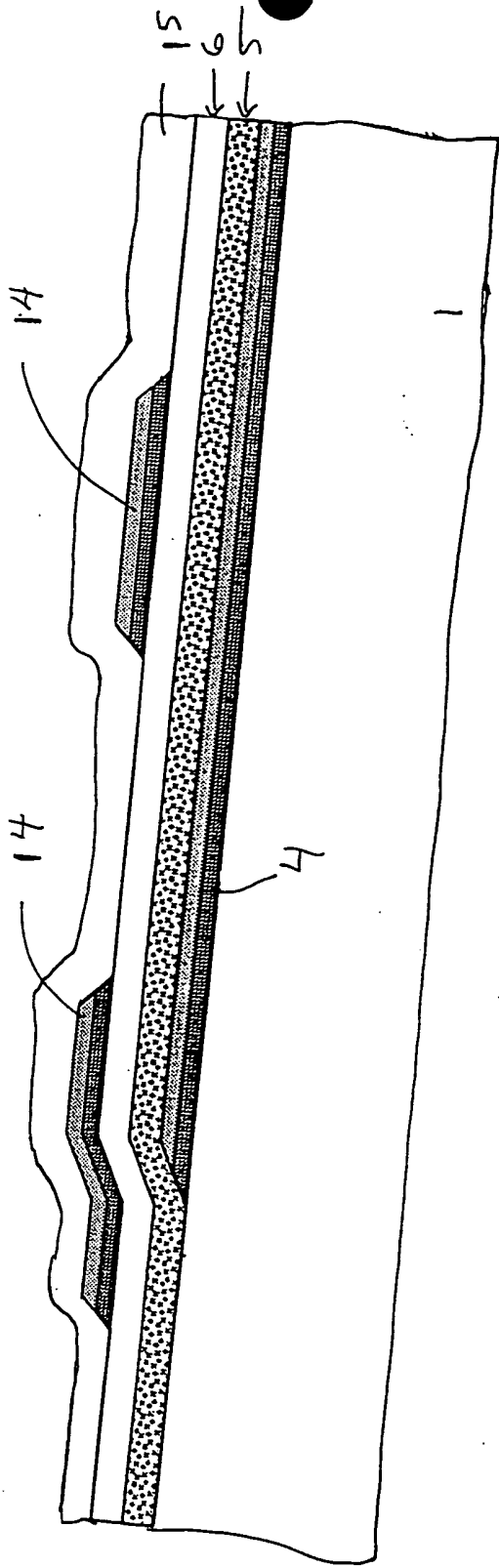


FIG. 10A

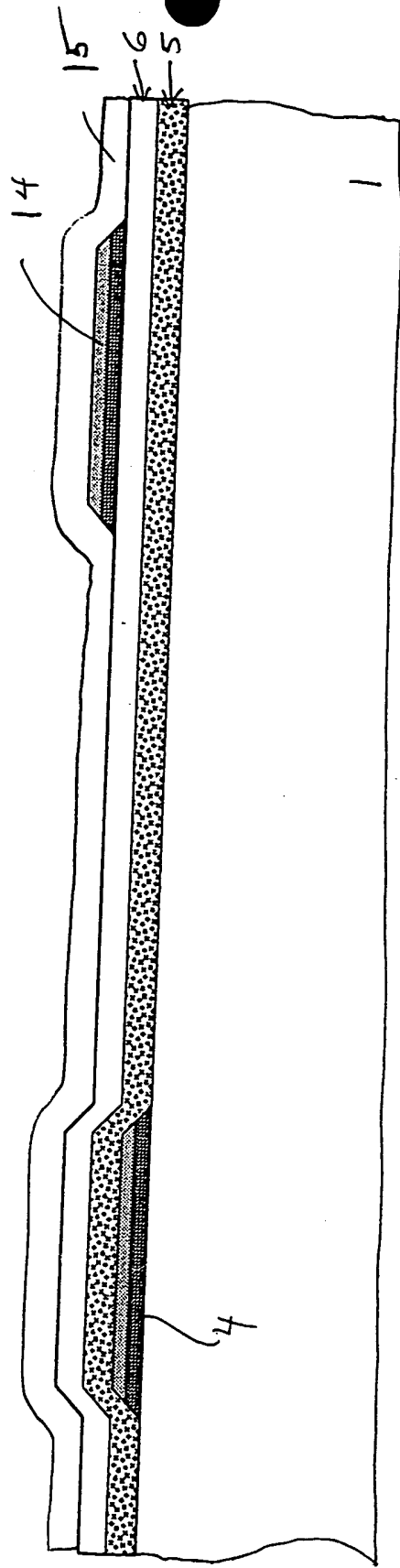


FIG. 10B

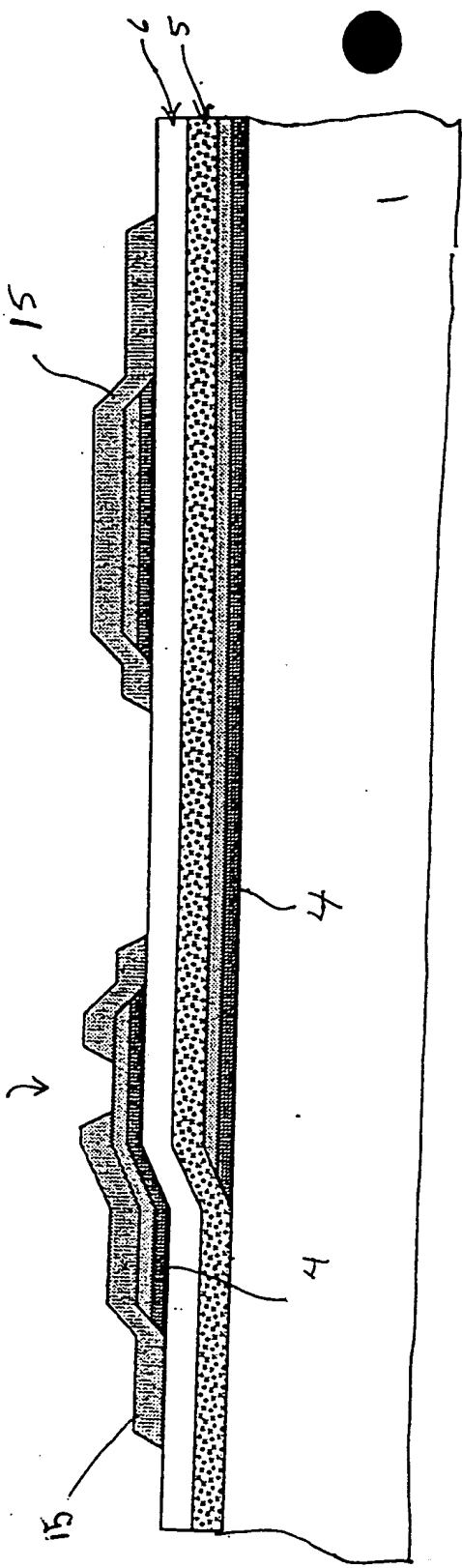


FIG. 11A

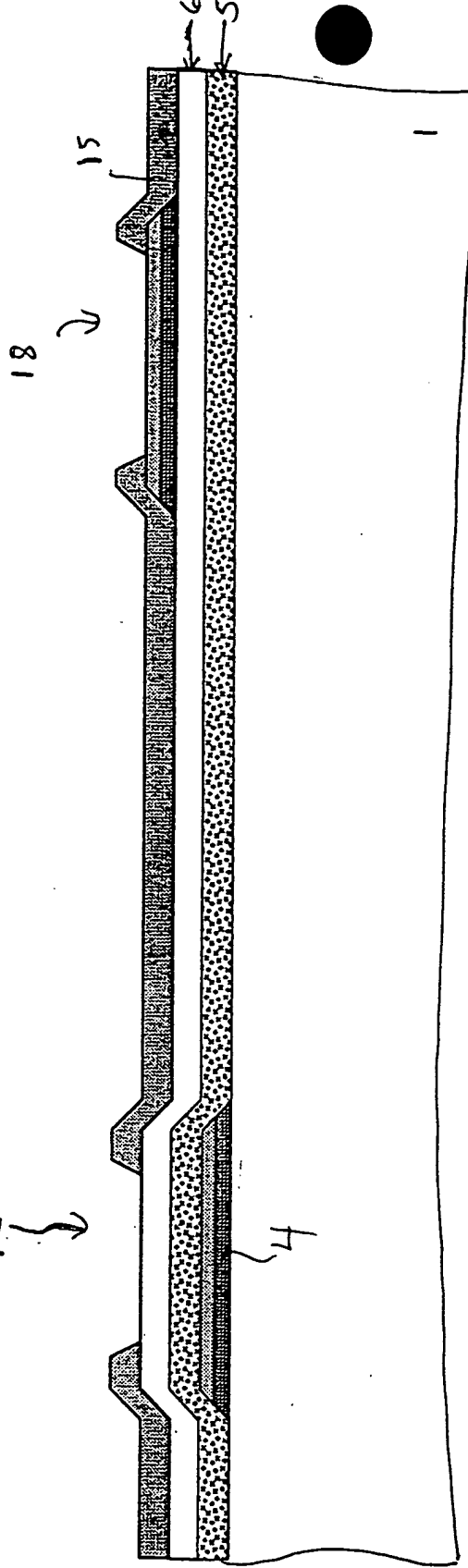


FIG. 11B

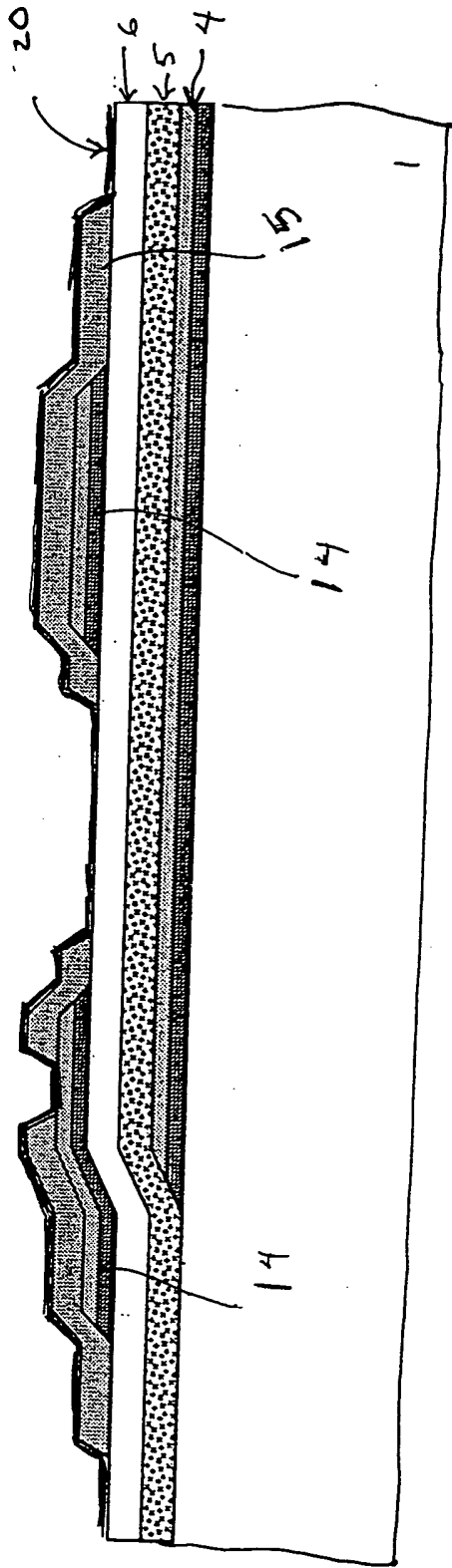


FIG. 12A

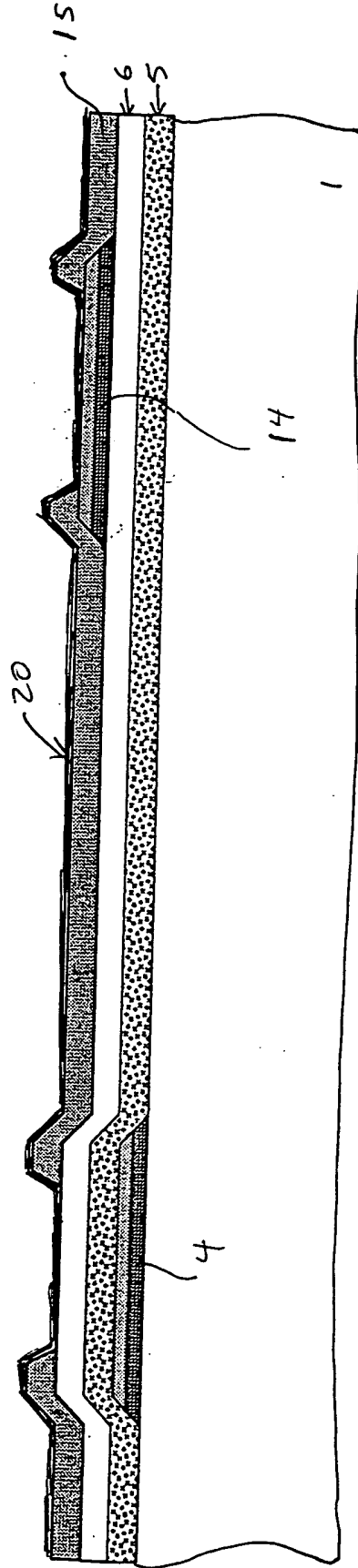


FIG. 12B

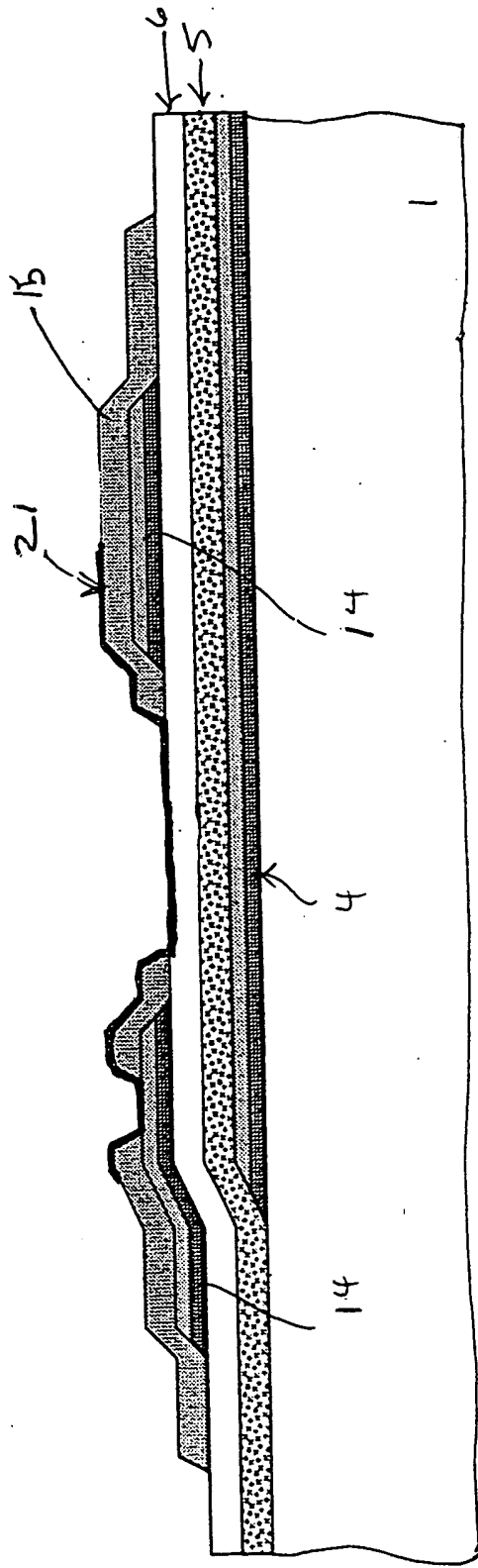


FIG. 13A

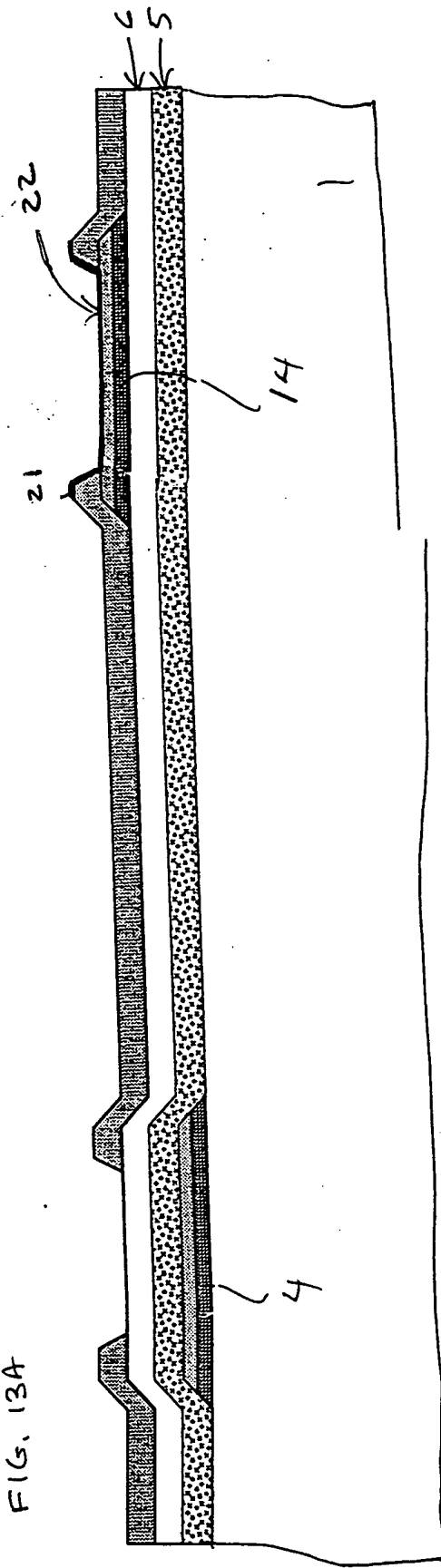


FIG. 13B

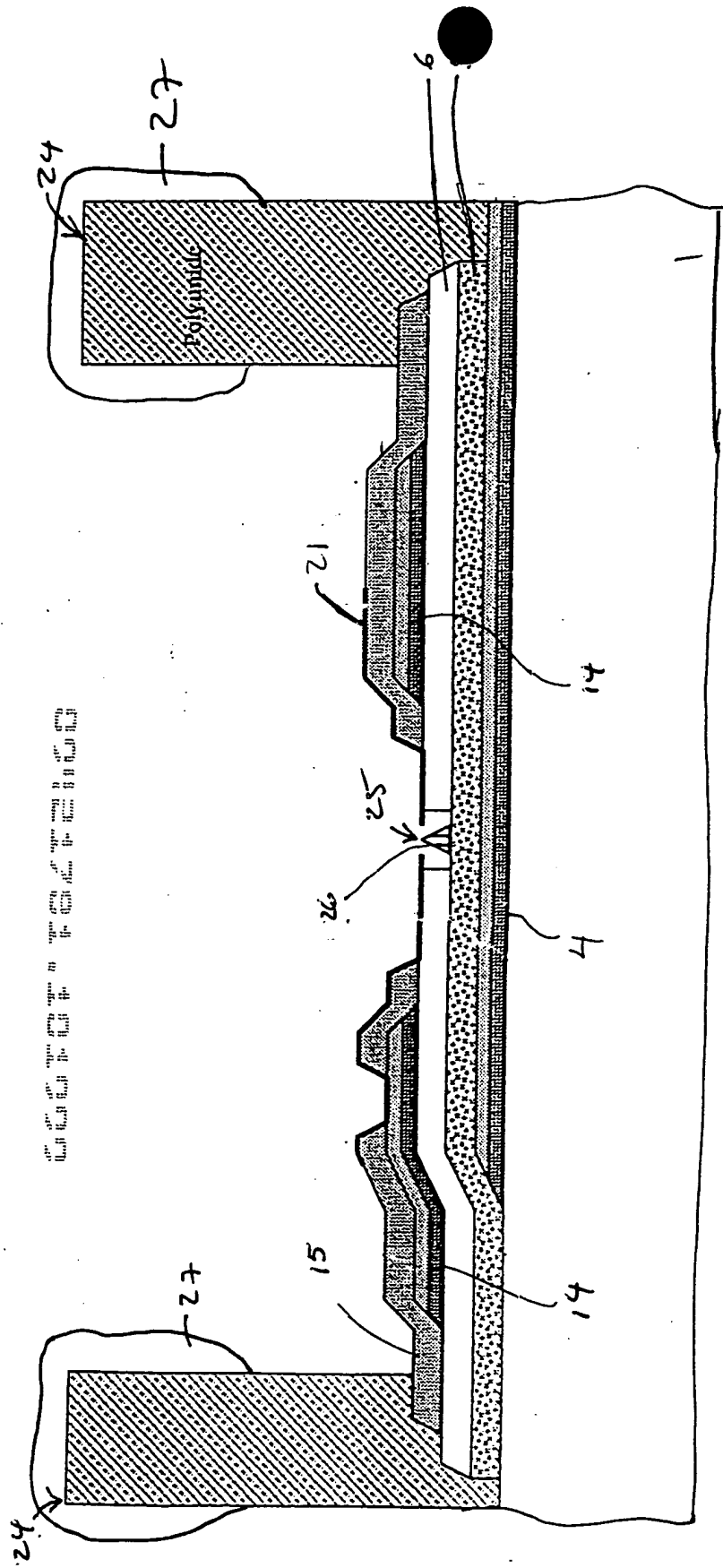


FIG. 14A

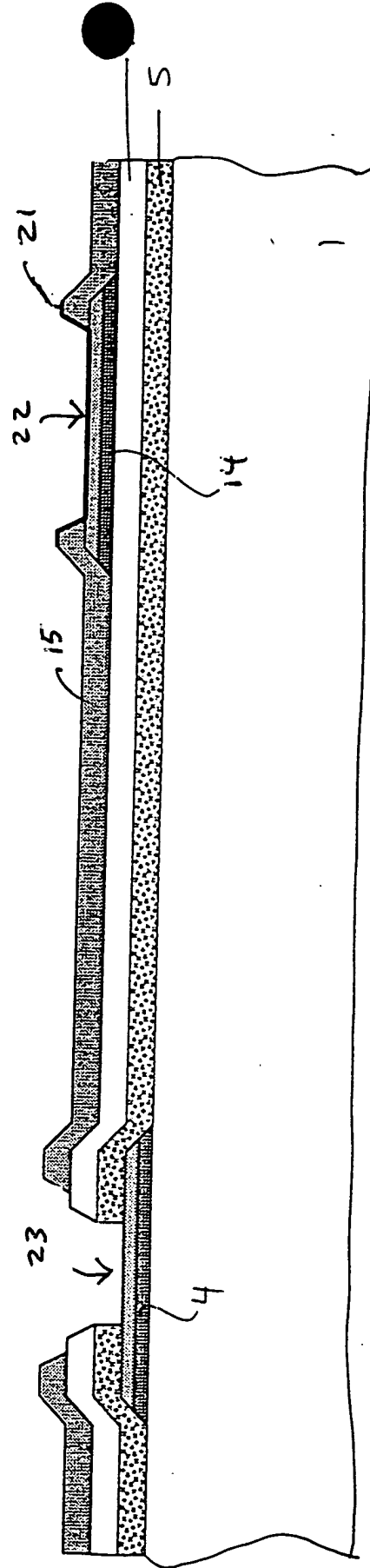


FIG. 14B

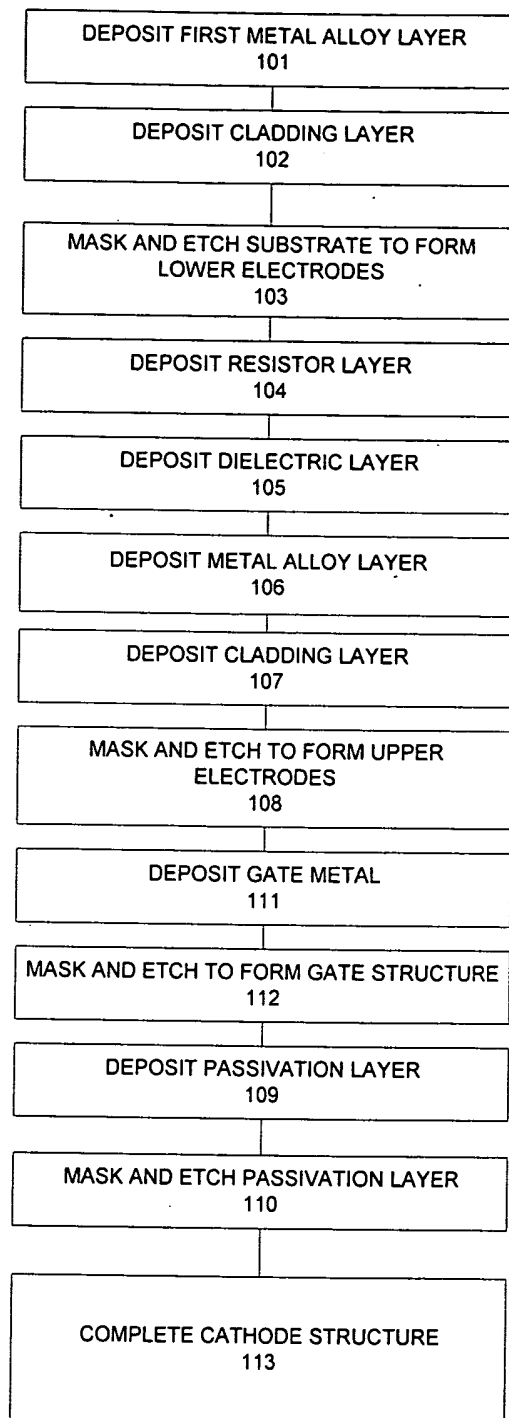


FIG. 15

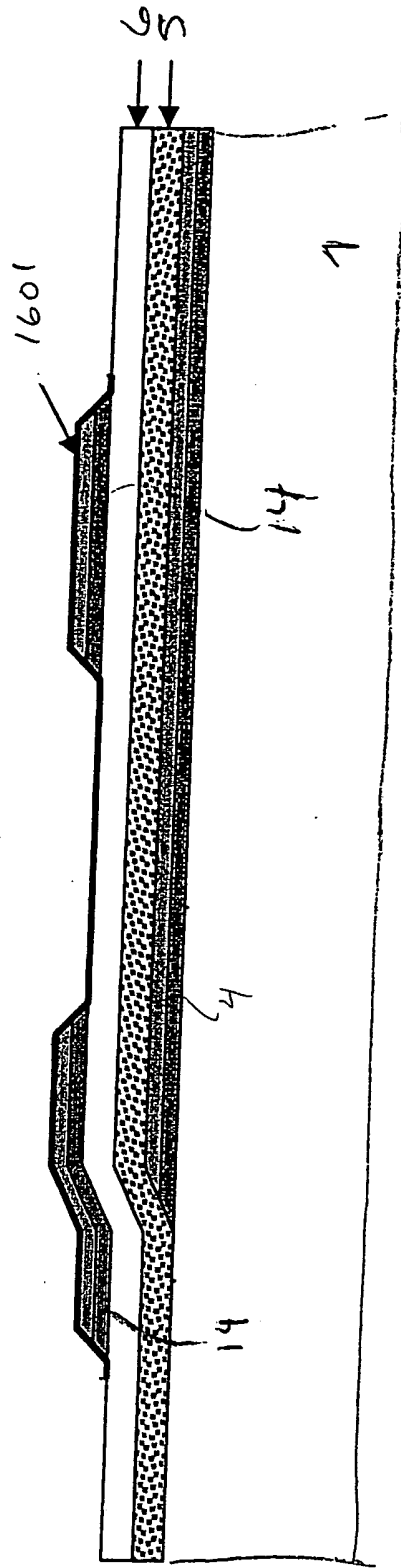


FIG. 16A

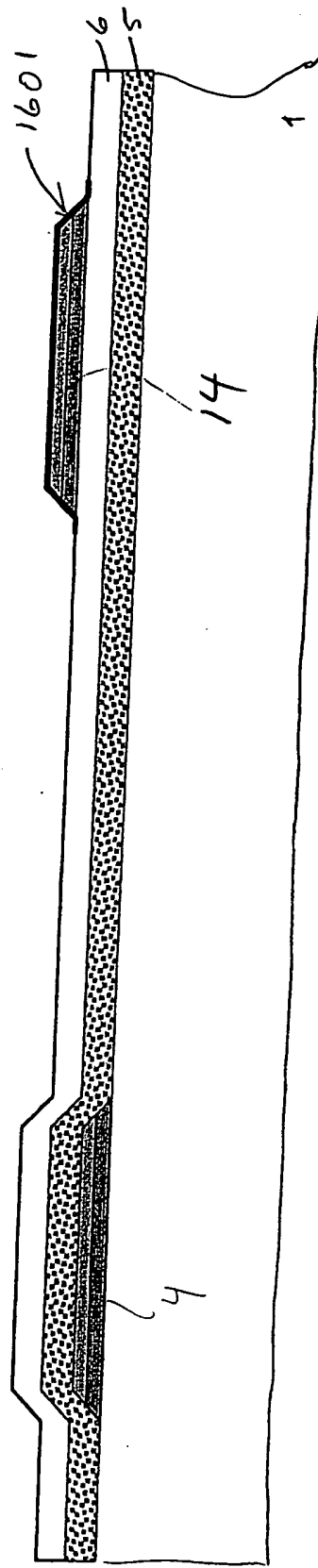


FIG. 16B

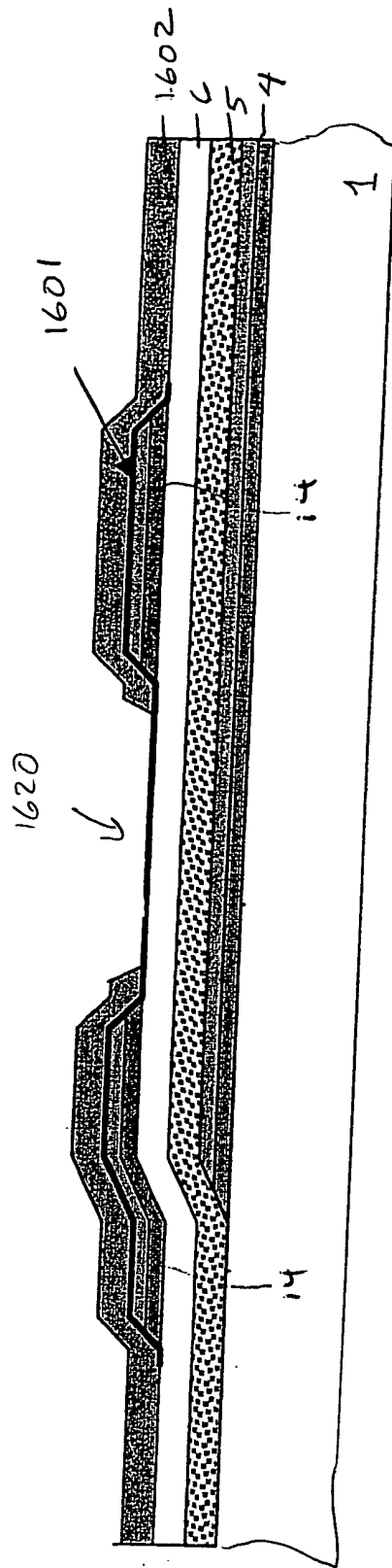


FIG. 16C

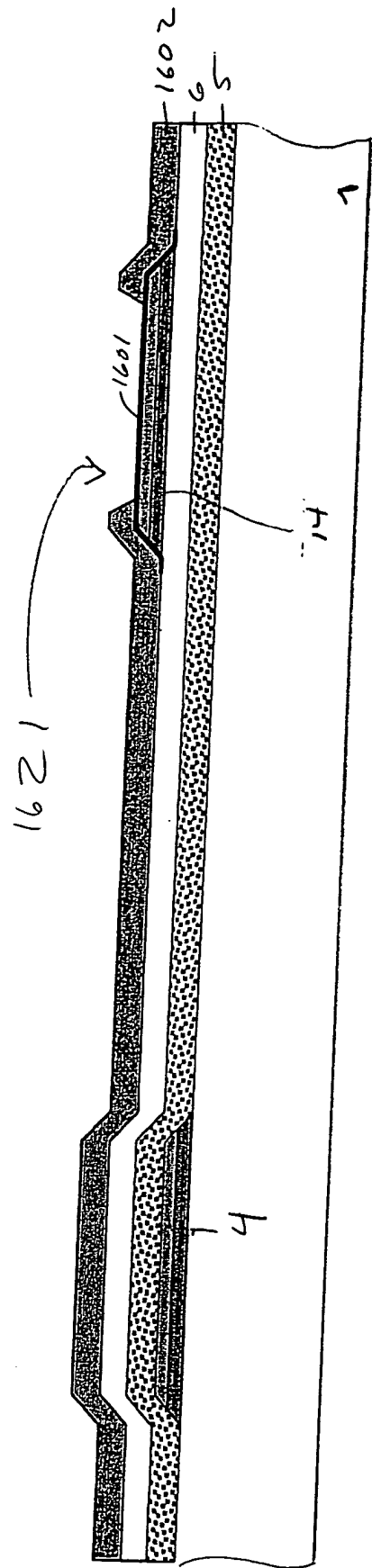


FIG. 16D

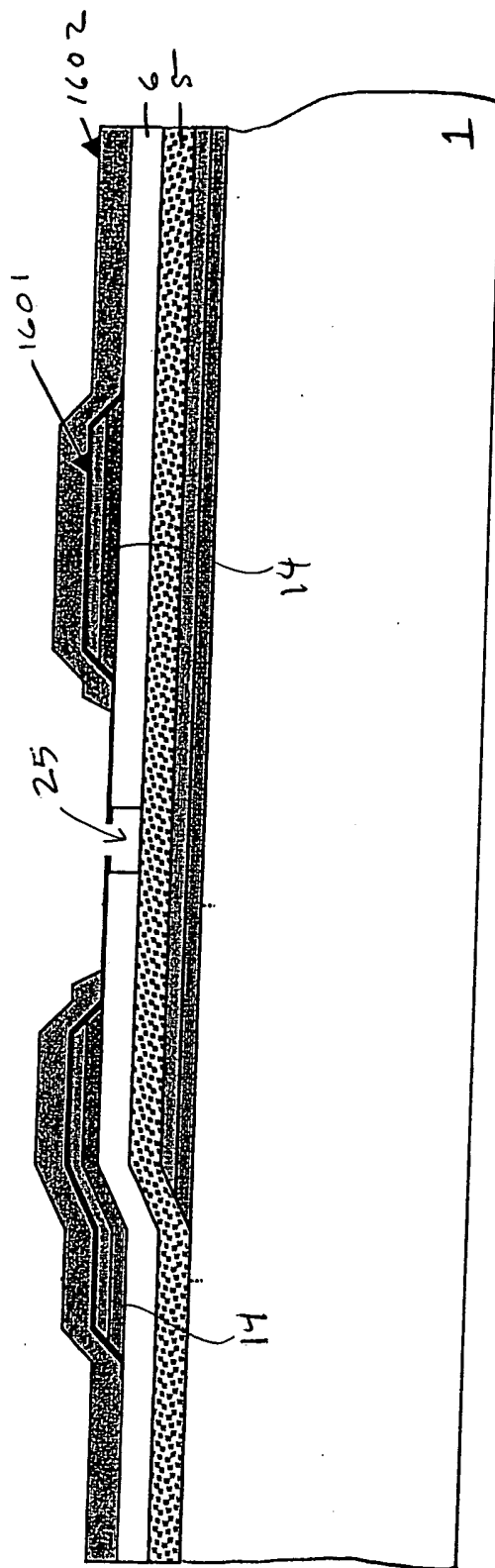


FIG. 16E

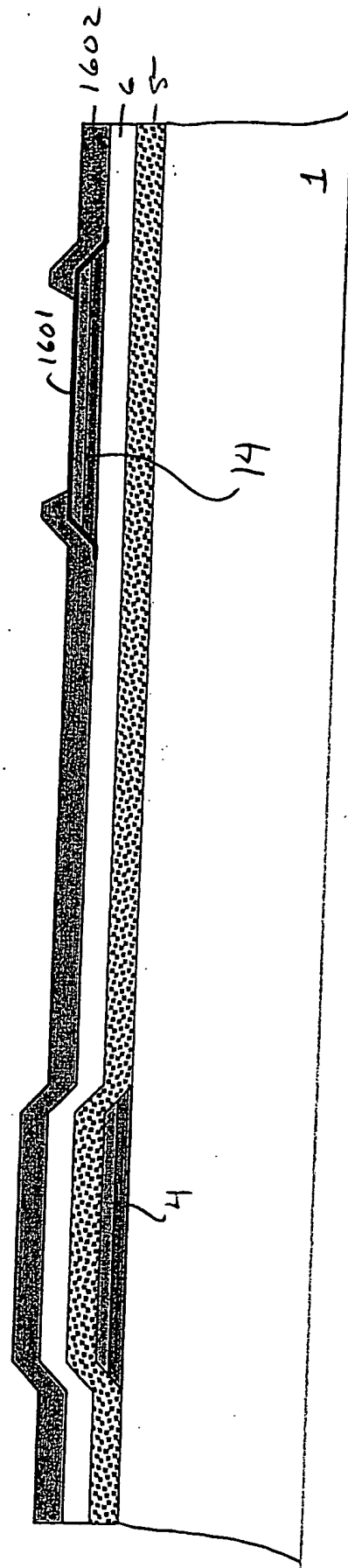


FIG. 16F

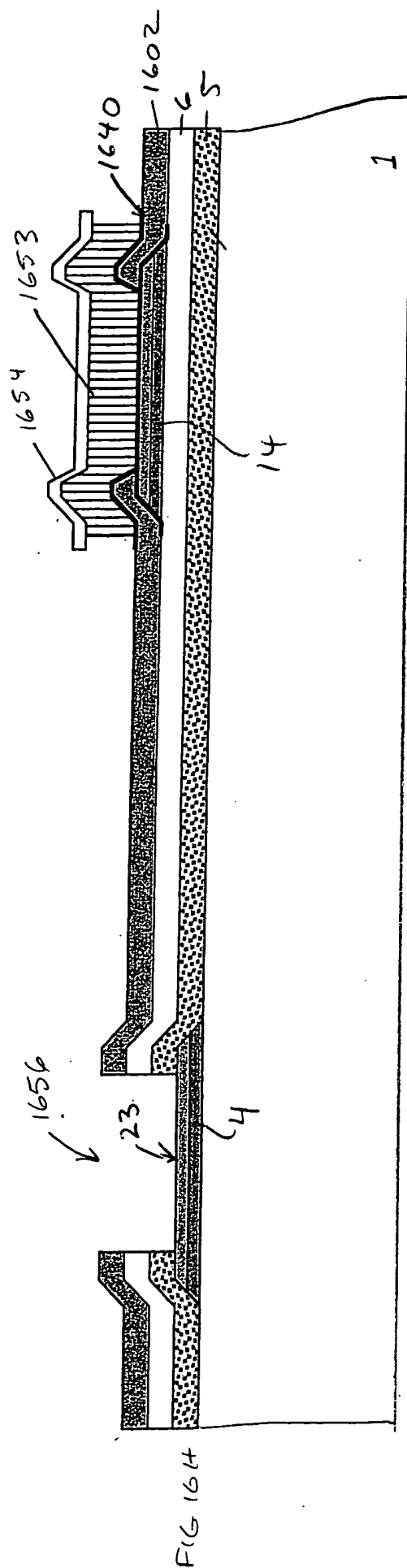
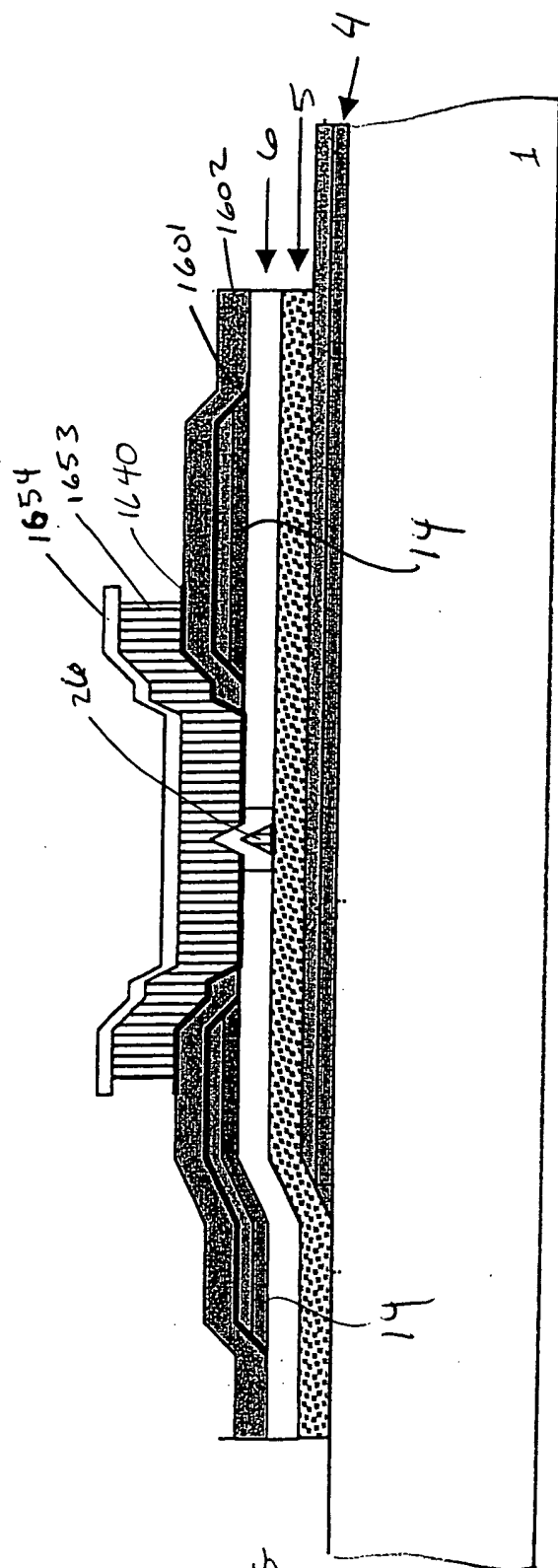


FIG. 16 I

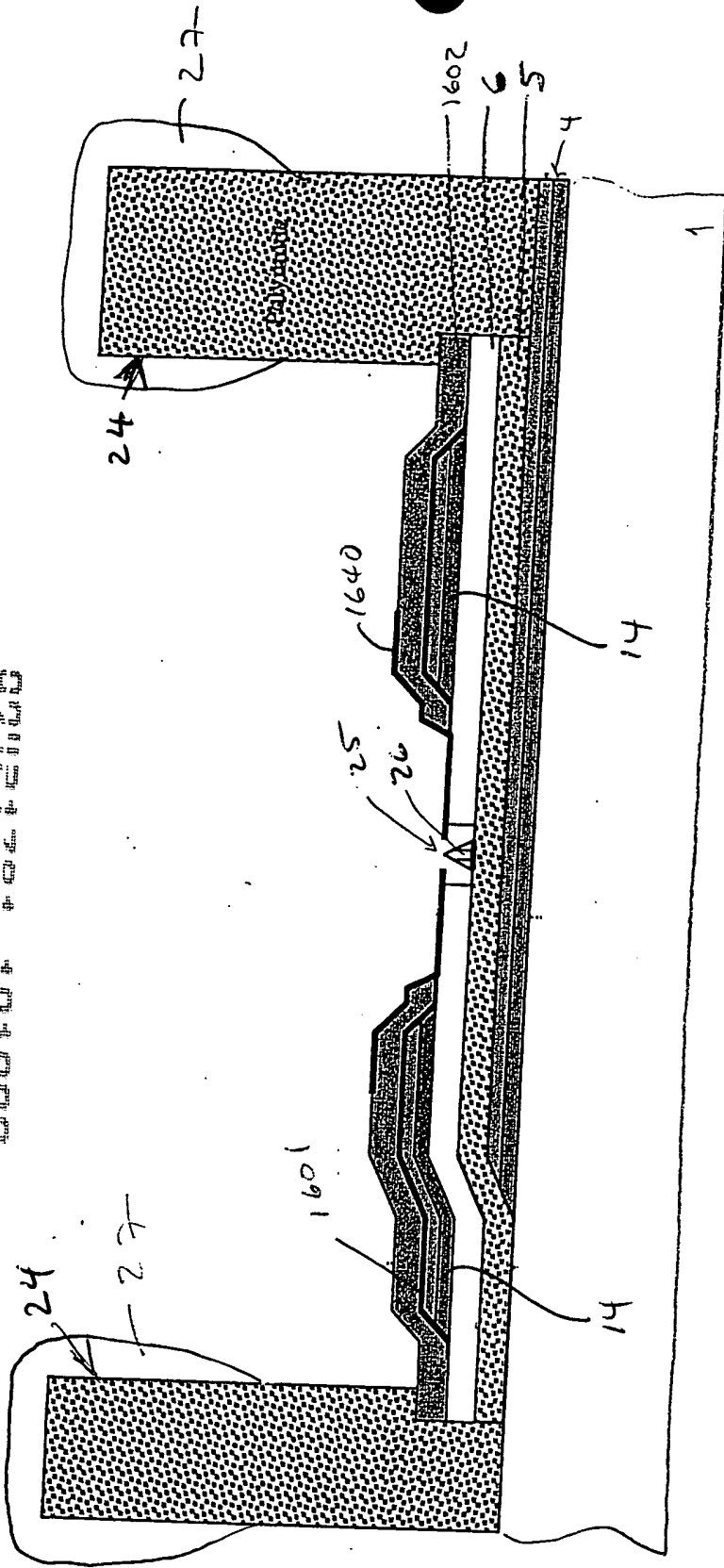


FIG 16 I

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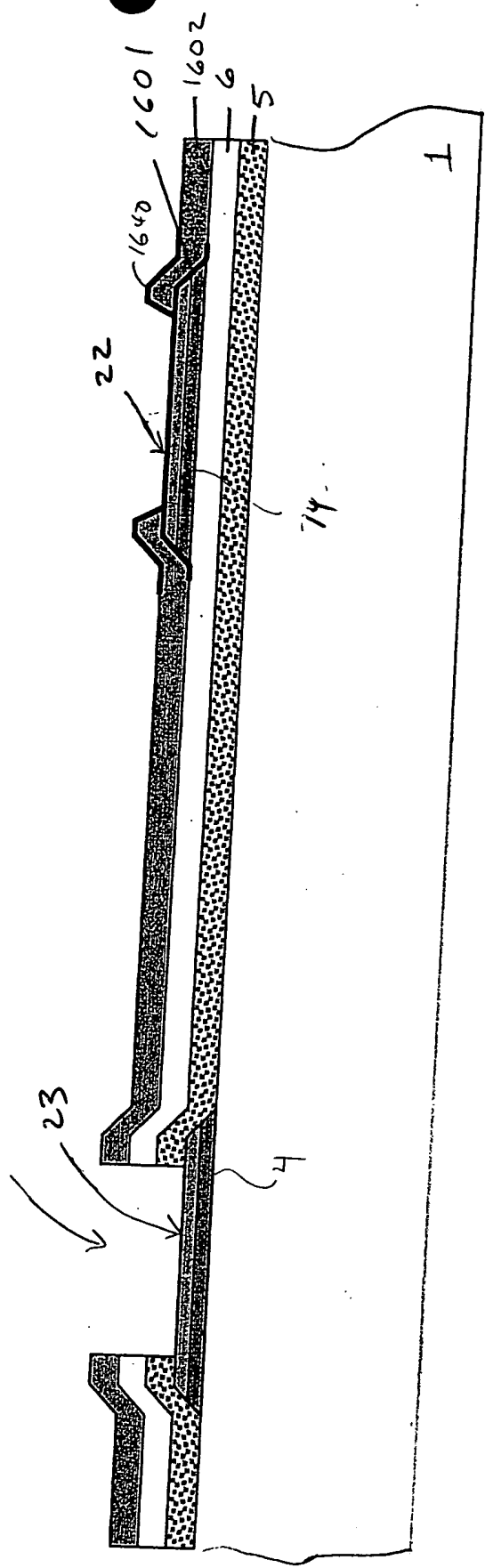


FIG 16 J

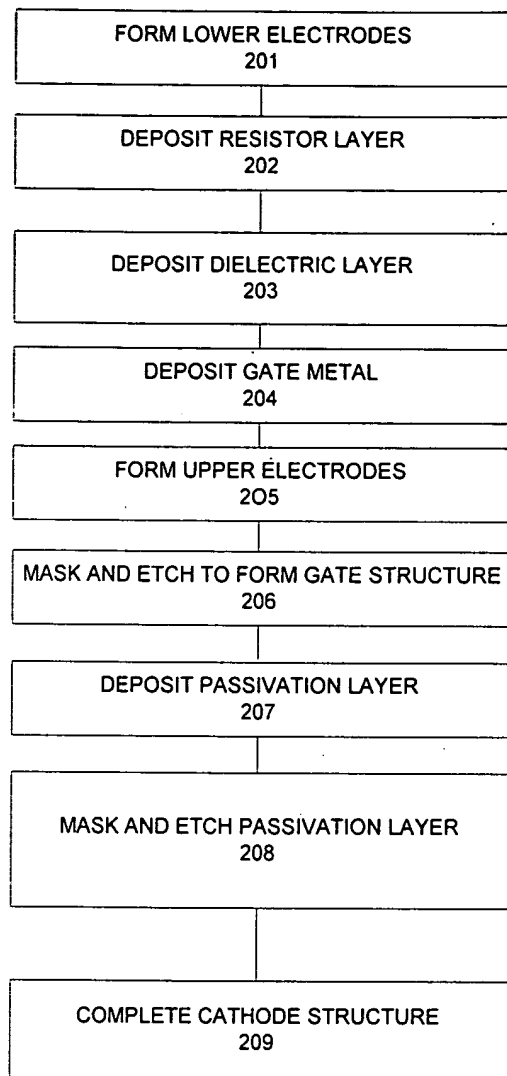
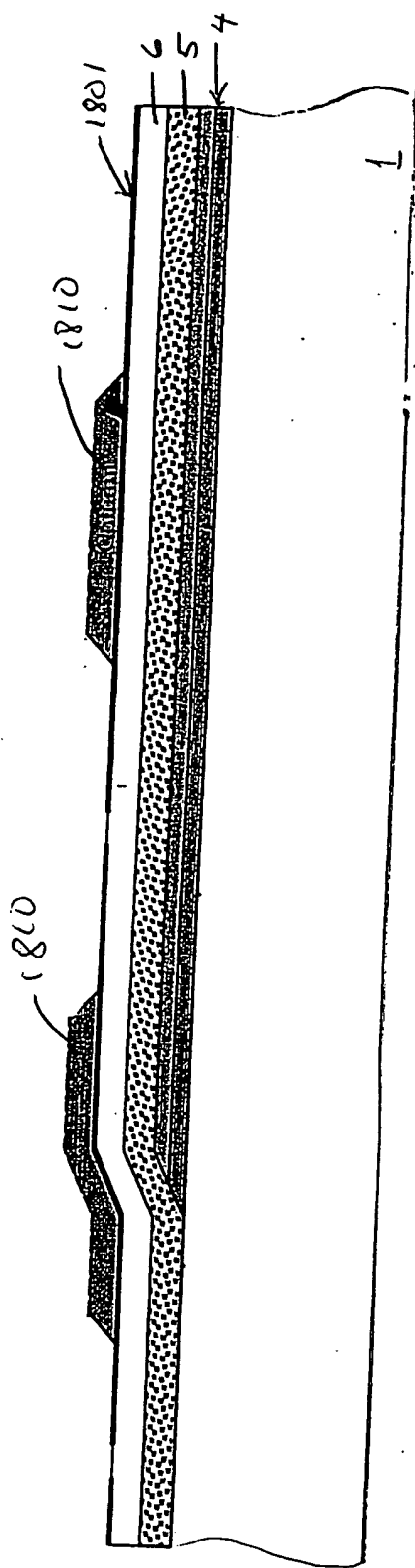


FIG. 17

[illegible]

4-5-84

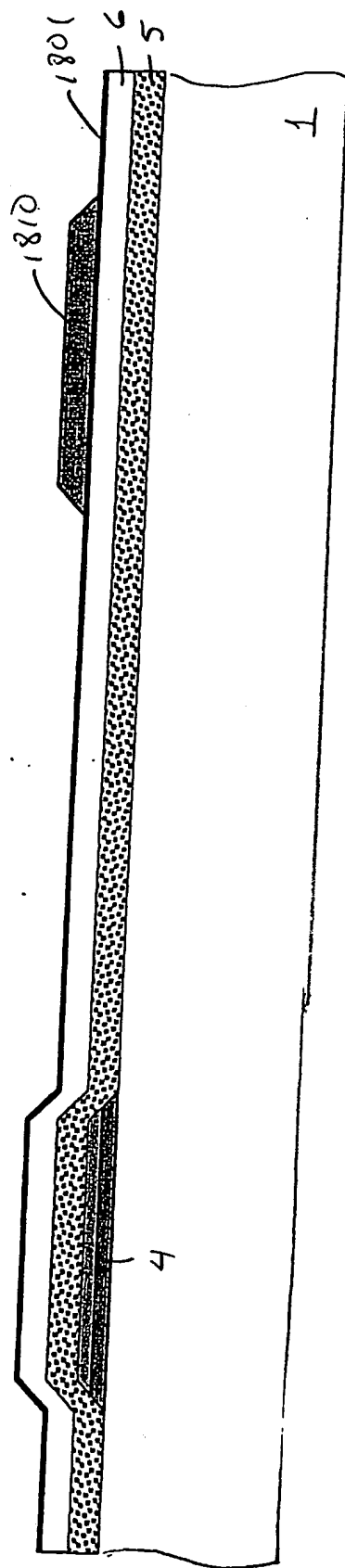


FIG. 18B

FIG. 18C is a cross-sectional view of a device 100, showing a substrate 10, a first layer 11, a second layer 12, a third layer 13, a fourth layer 14, a fifth layer 15, a sixth layer 16, a seventh layer 17, an eighth layer 18, a ninth layer 19, a tenth layer 20, an eleventh layer 21, a twelfth layer 22, a thirteenth layer 23, a fourteenth layer 24, a fifteenth layer 25, a sixteenth layer 26, a seventeenth layer 27, an eighteenth layer 28, a nineteenth layer 29, a twentieth layer 30, a twenty-first layer 31, a twenty-second layer 32, a twenty-third layer 33, a twenty-fourth layer 34, a twenty-fifth layer 35, a twenty-sixth layer 36, a twenty-seventh layer 37, a twenty-eighth layer 38, a twenty-ninth layer 39, a thirtieth layer 40, a thirty-first layer 41, a thirty-second layer 42, a thirty-third layer 43, a thirty-fourth layer 44, a thirty-fifth layer 45, a thirty-sixth layer 46, a thirty-seventh layer 47, a thirty-eighth layer 48, a thirty-ninth layer 49, a fortieth layer 50, a forty-first layer 51, a forty-second layer 52, a forty-third layer 53, a forty-fourth layer 54, a forty-fifth layer 55, a forty-sixth layer 56, a forty-seventh layer 57, a forty-eighth layer 58, a forty-ninth layer 59, a fiftieth layer 60, a fifty-first layer 61, a fifty-second layer 62, a fifty-third layer 63, a fifty-fourth layer 64, a fifty-fifth layer 65, a fifty-sixth layer 66, a fifty-seventh layer 67, a fifty-eighth layer 68, a fifty-ninth layer 69, a sixtieth layer 70, a sixty-first layer 71, a sixty-second layer 72, a sixty-third layer 73, a sixty-fourth layer 74, a sixty-fifth layer 75, a sixty-sixth layer 76, a sixty-seventh layer 77, a sixty-eighth layer 78, a sixty-ninth layer 79, a seventieth layer 80, a seventy-first layer 81, a seventy-second layer 82, a seventy-third layer 83, a seventy-fourth layer 84, a seventy-fifth layer 85, a seventy-sixth layer 86, a seventy-seventh layer 87, a seventy-eighth layer 88, a seventy-ninth layer 89, an eightieth layer 90, an eighty-first layer 91, an eighty-second layer 92, an eighty-third layer 93, an eighty-fourth layer 94, an eighty-fifth layer 95, an eighty-sixth layer 96, an eighty-seventh layer 97, an eighty-eighth layer 98, an eighty-ninth layer 99, a ninetieth layer 100.

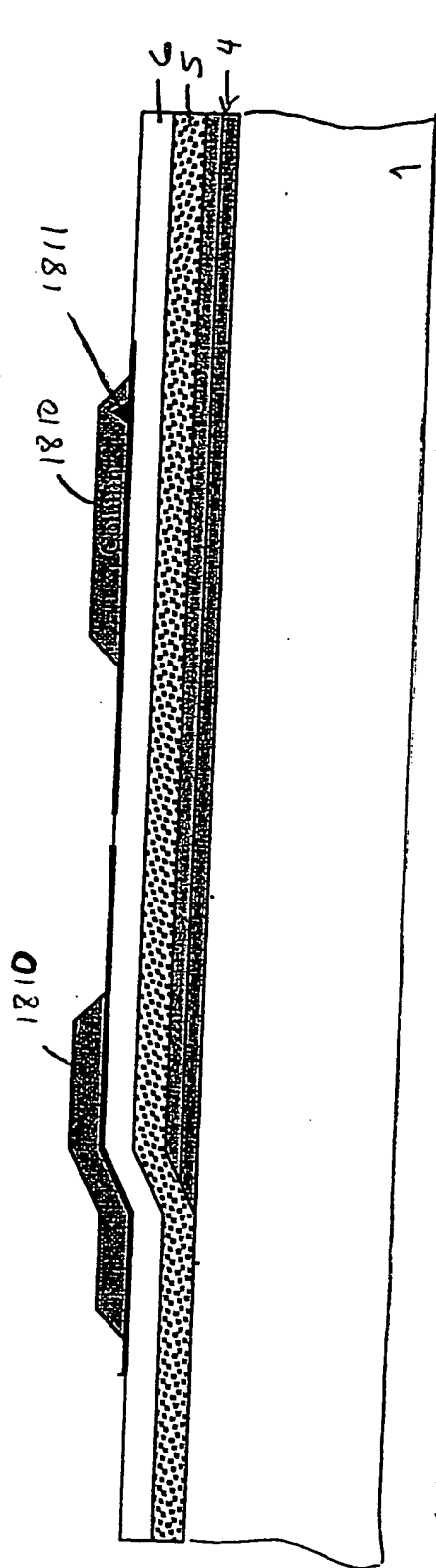


FIG. 18C

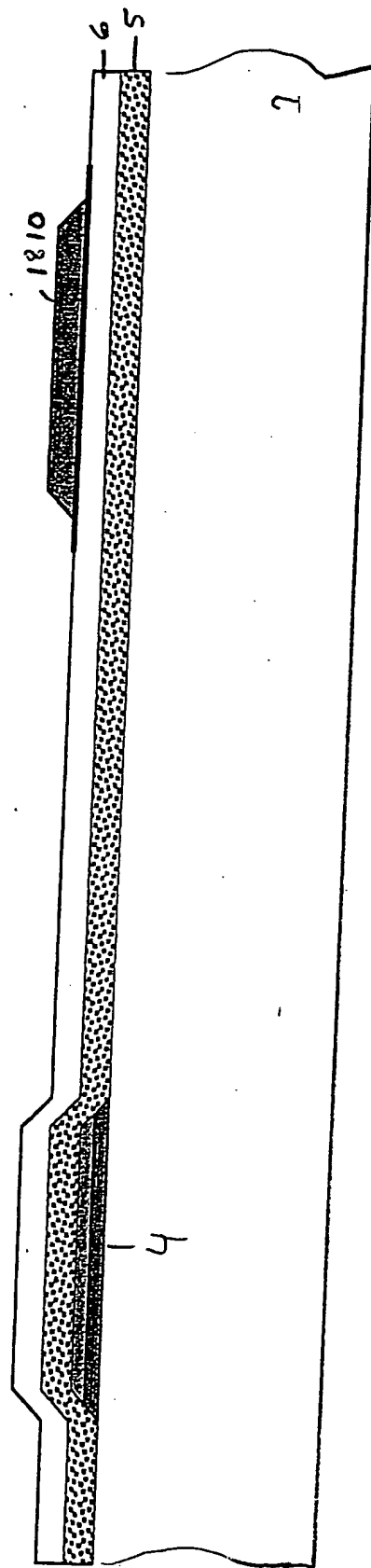


FIG. 18D

1820

1810

1811

1811

1830

6

5

4

1

18E

1281

1811

1830

6

5

1811

1

4

FIG. 18F

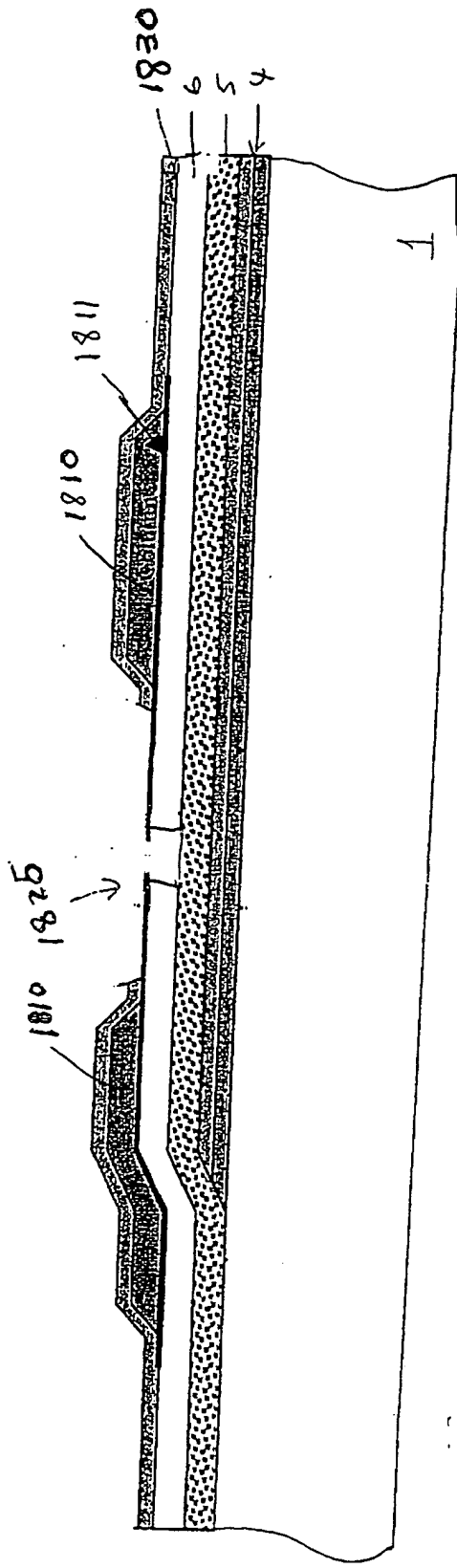


FIG. 18G

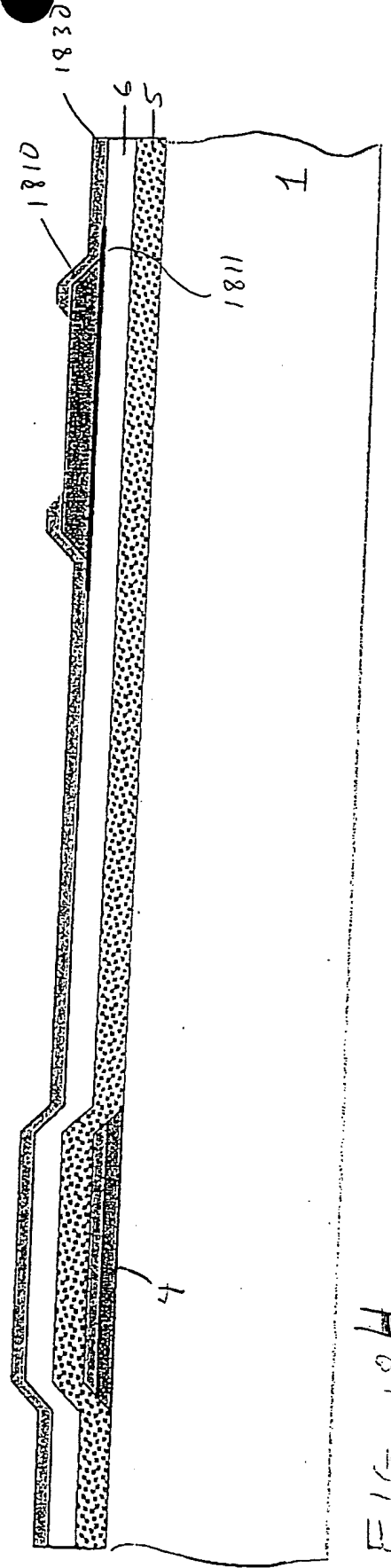
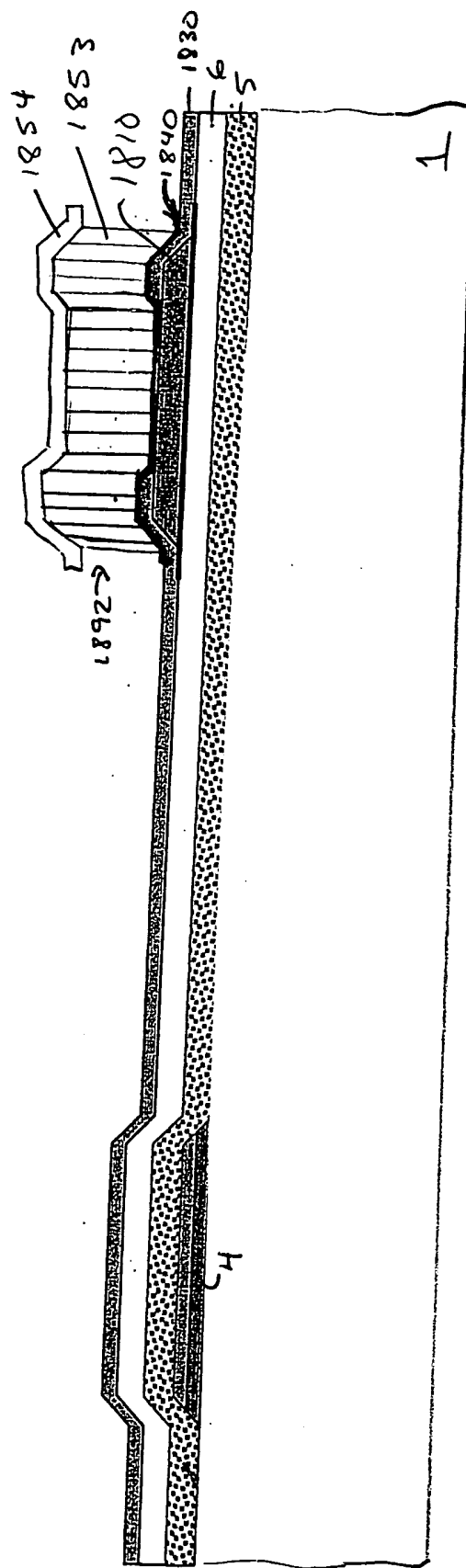
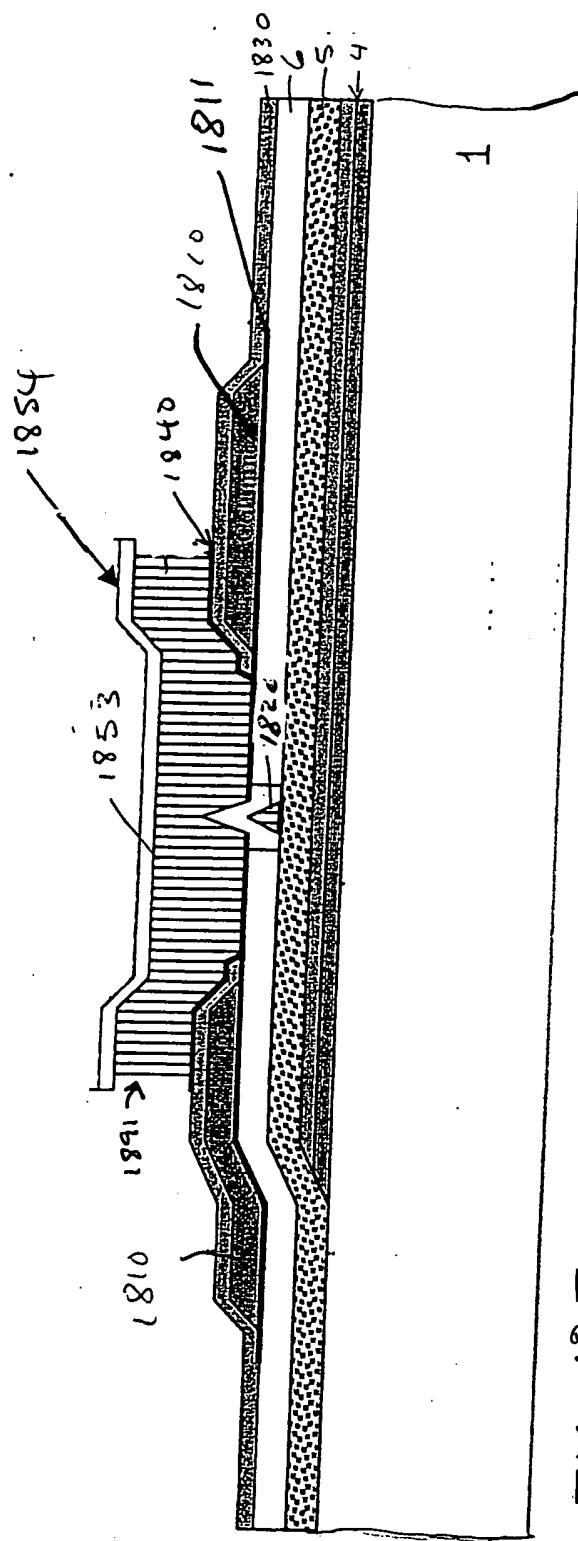


FIG. 18H



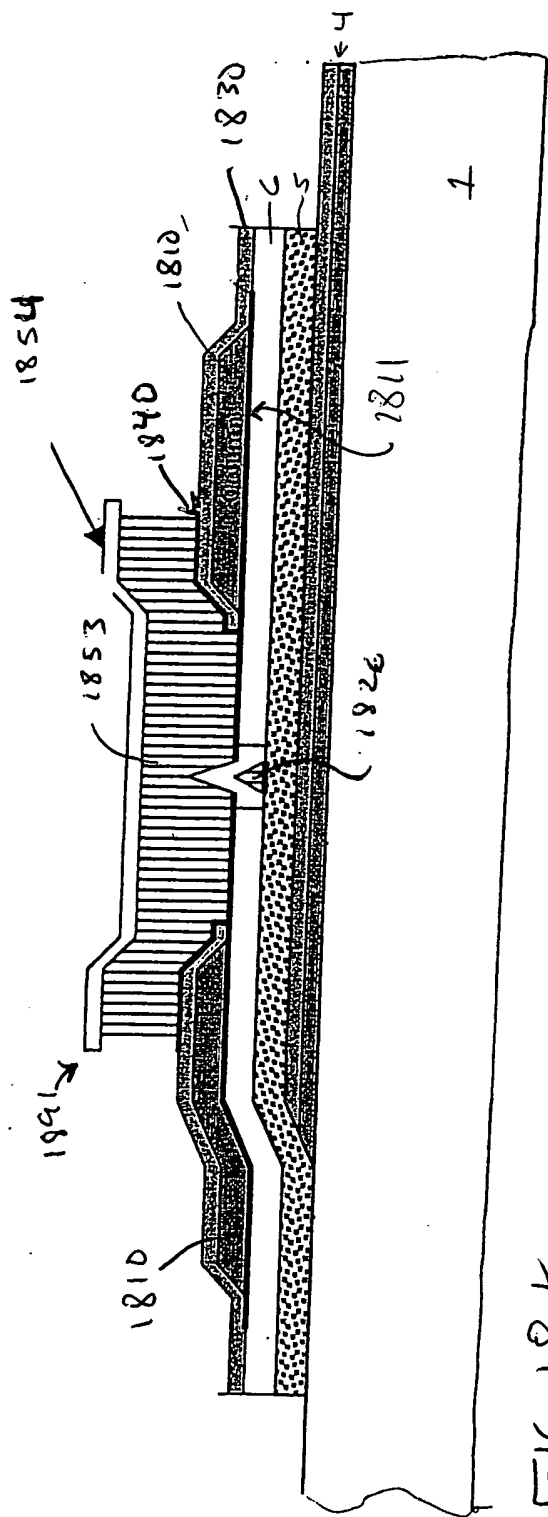


FIG 18 K

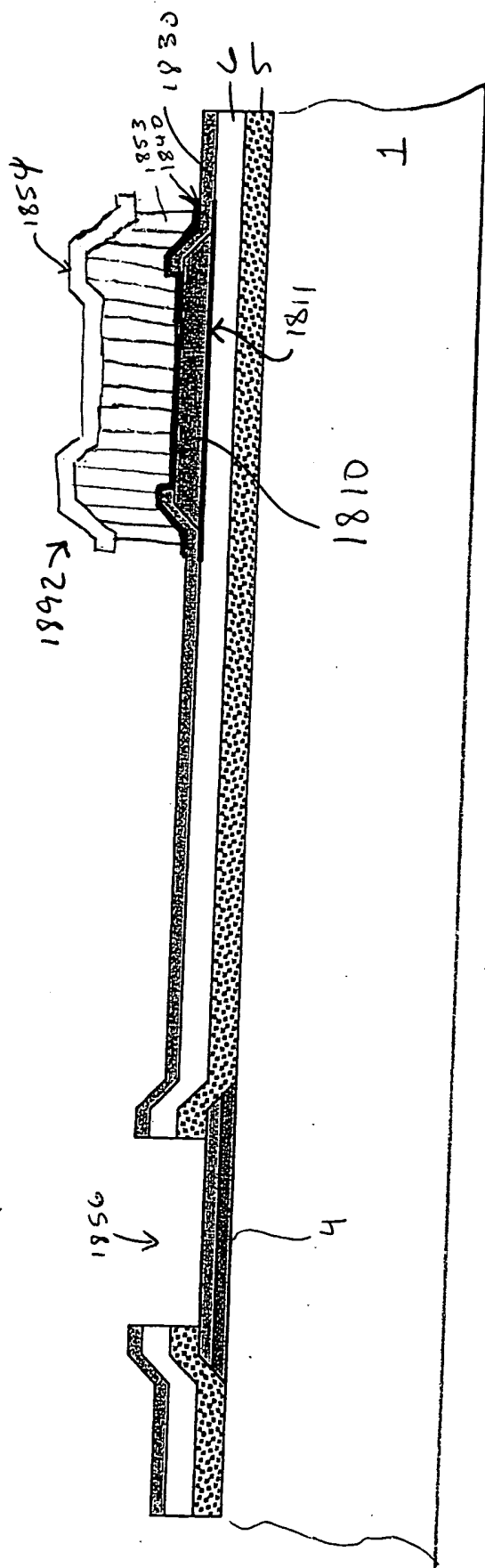


FIG 18 L

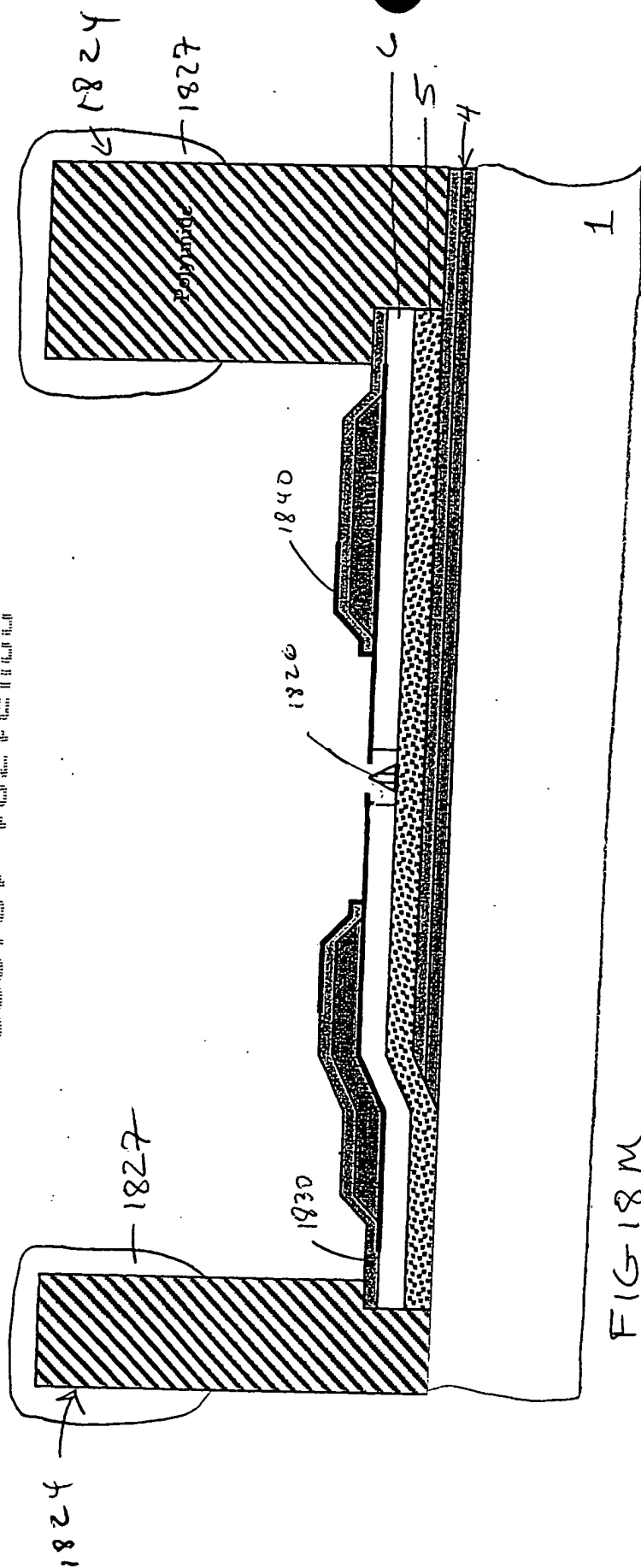
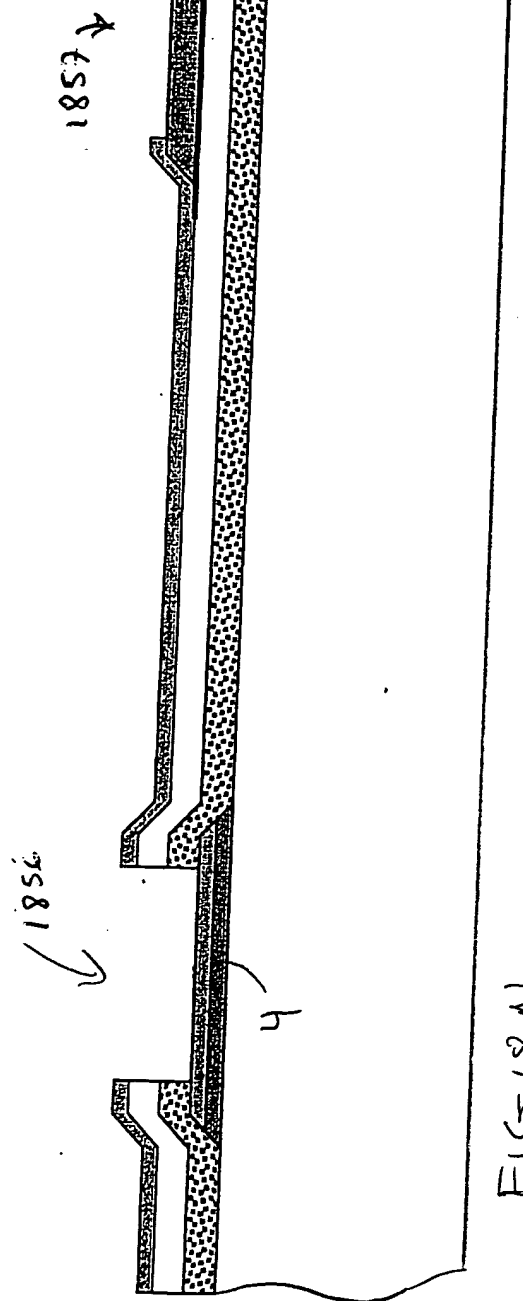


FIG-18M



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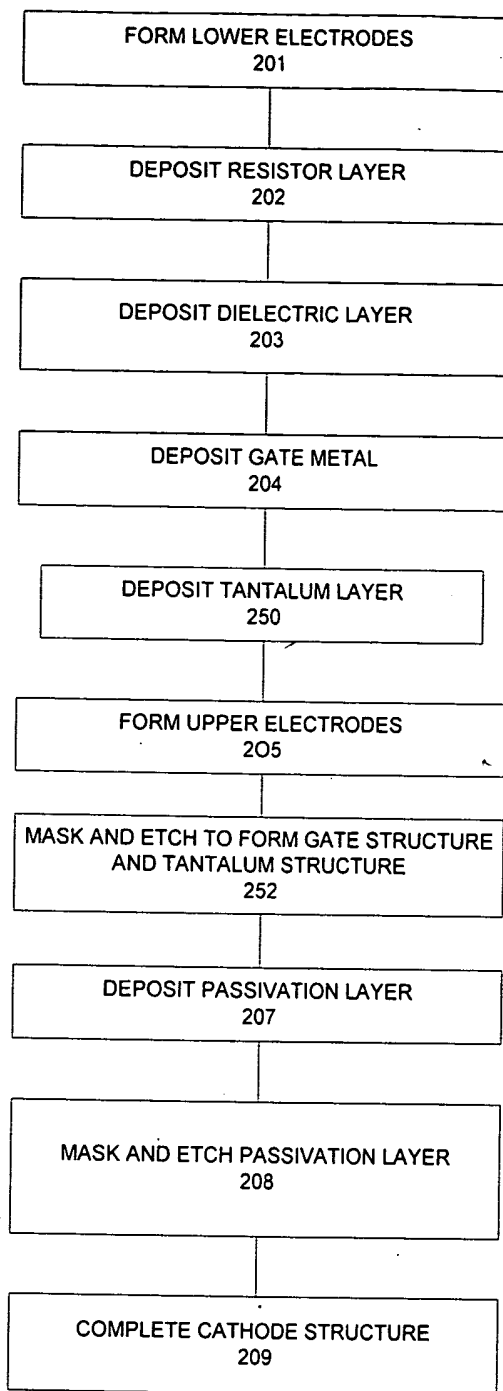


FIG. 19

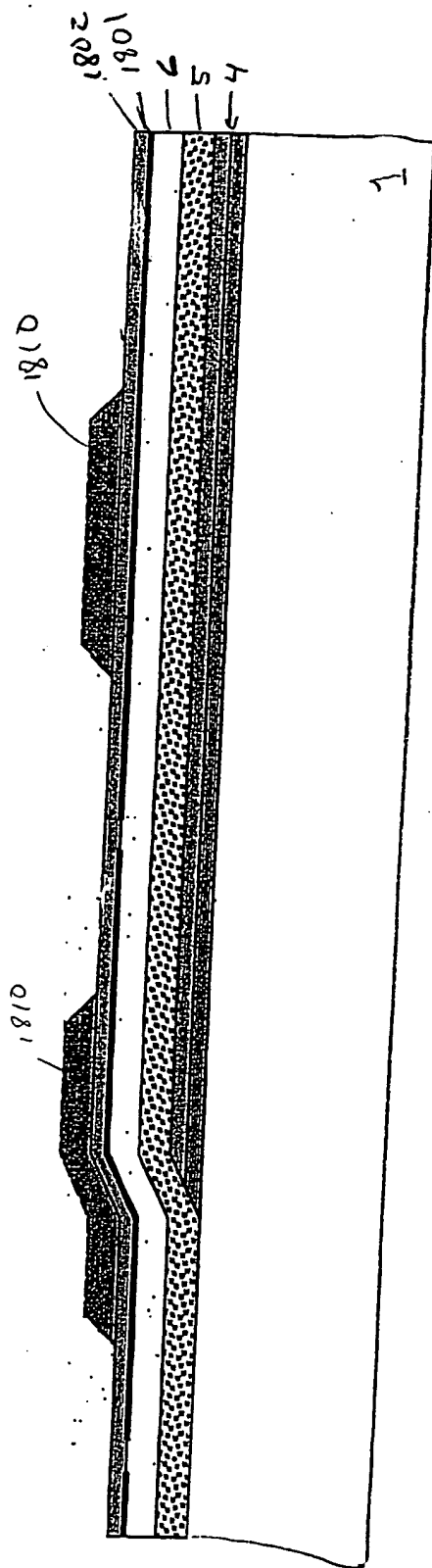


FIG. 20A

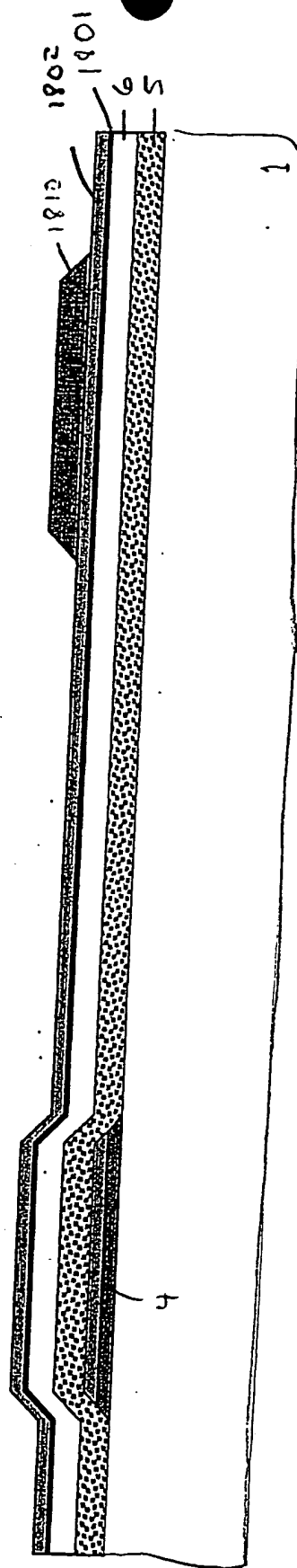


FIG. 20B

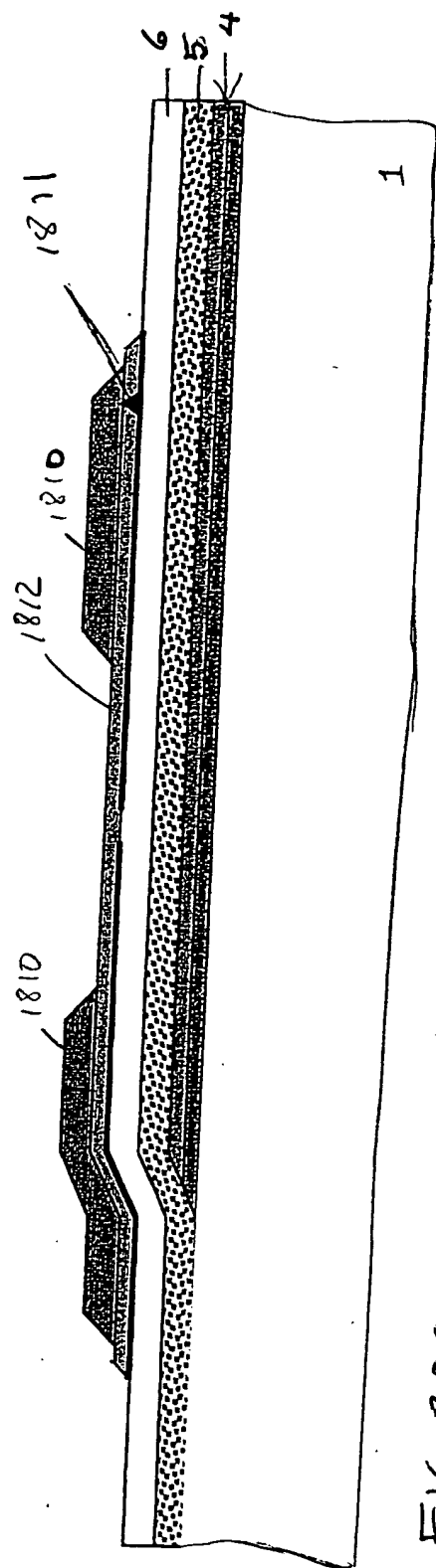


FIG. 20C

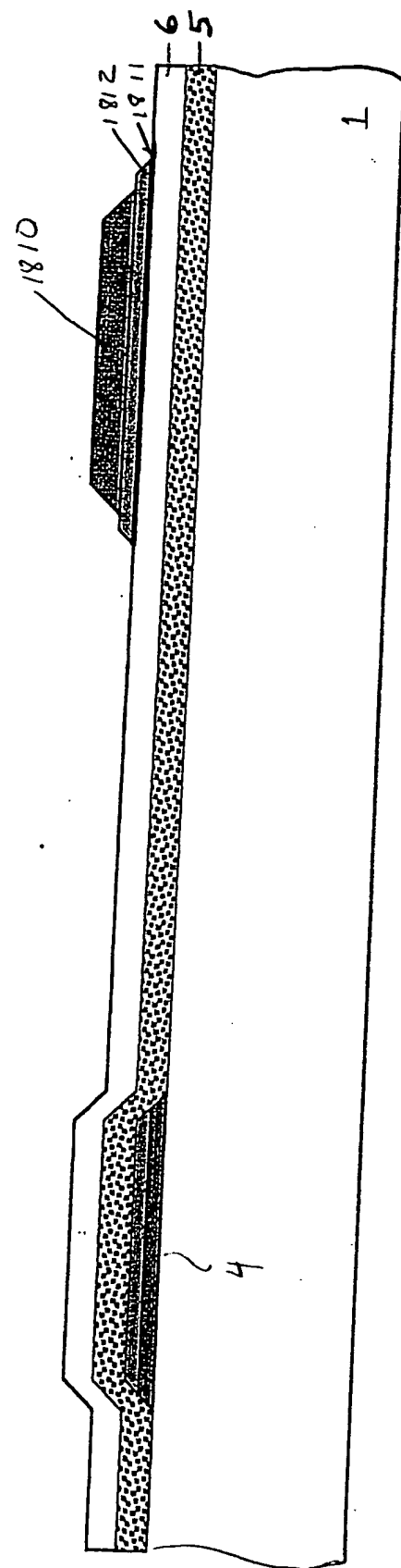


FIG. 20D

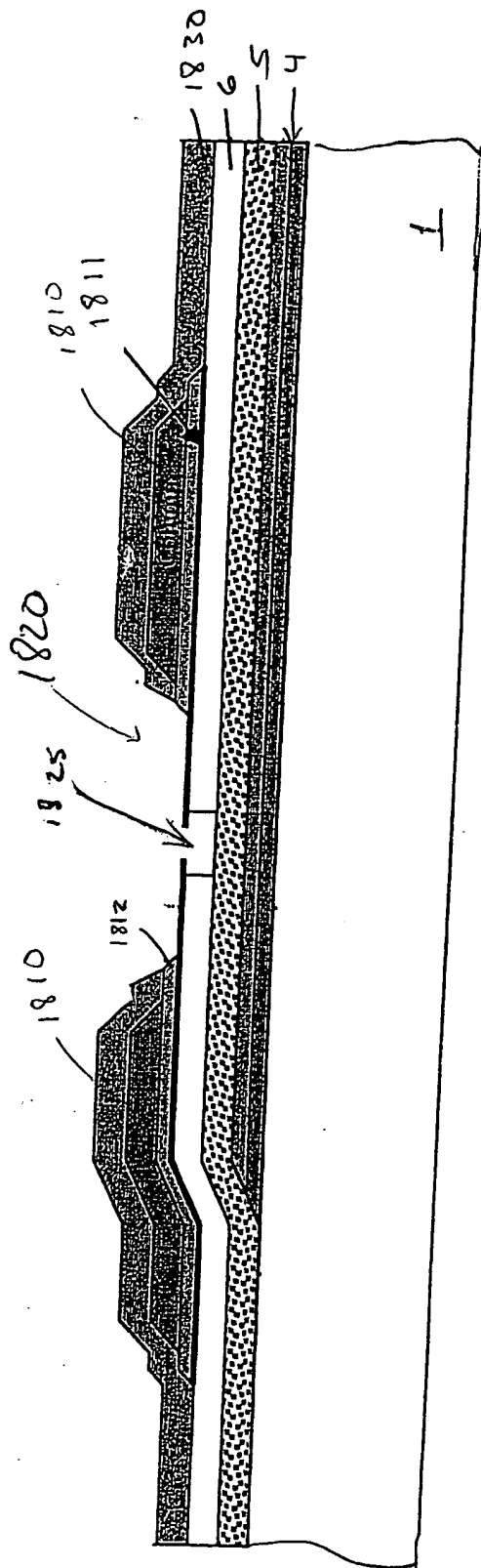


FIG 20E

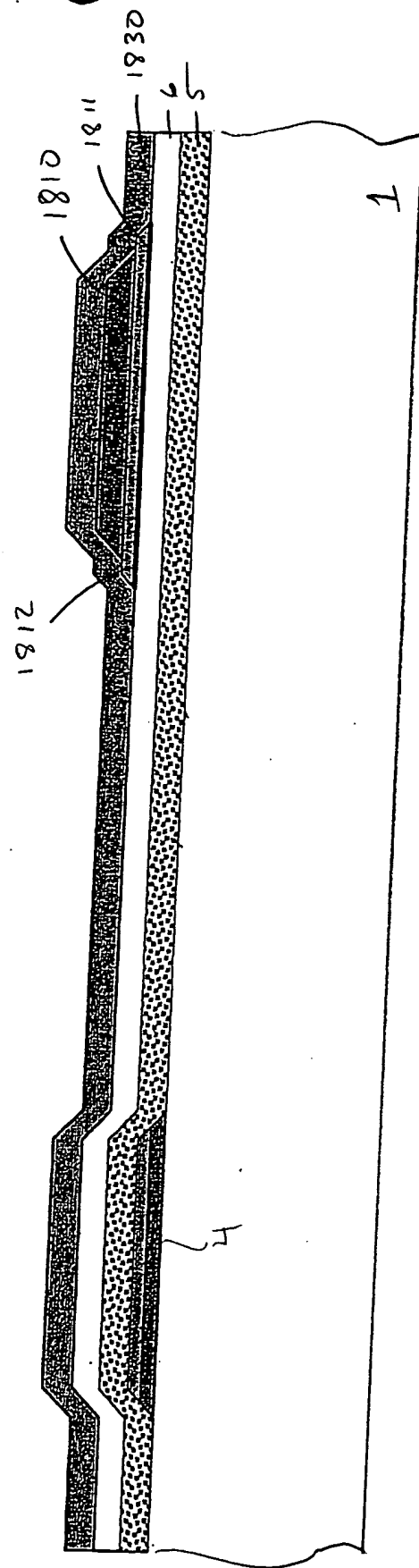


FIG 20F

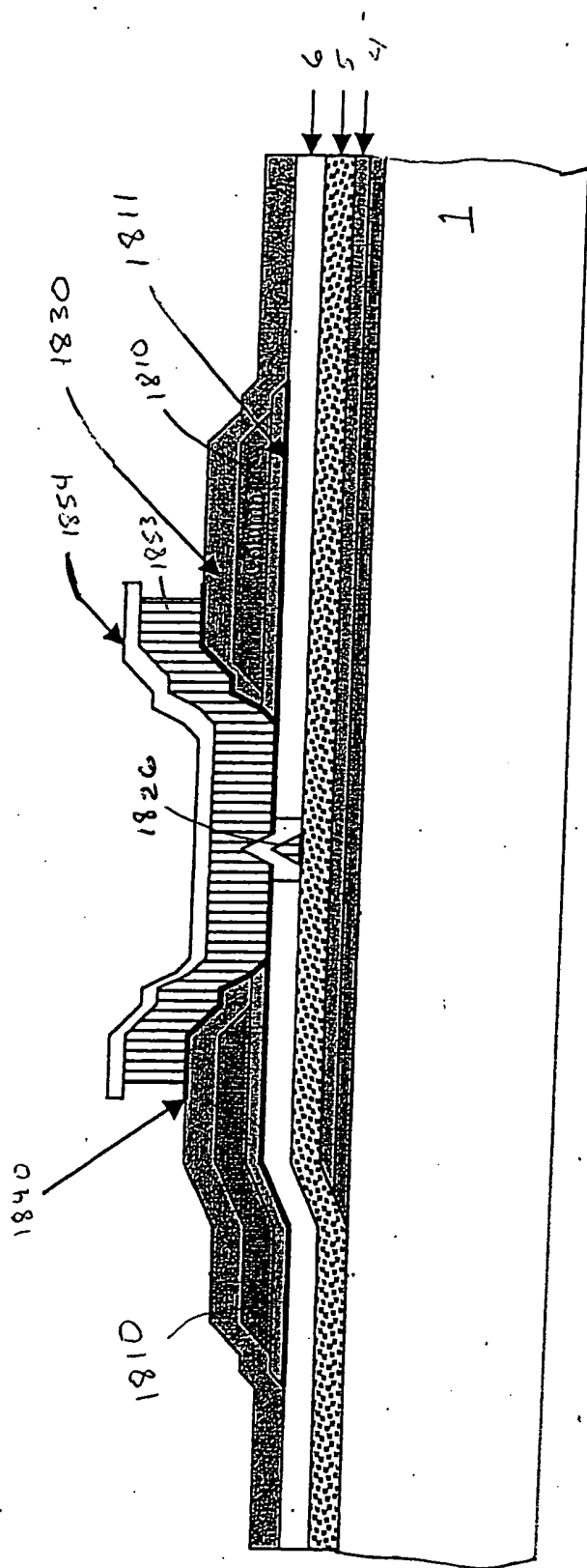


FIG. 20G

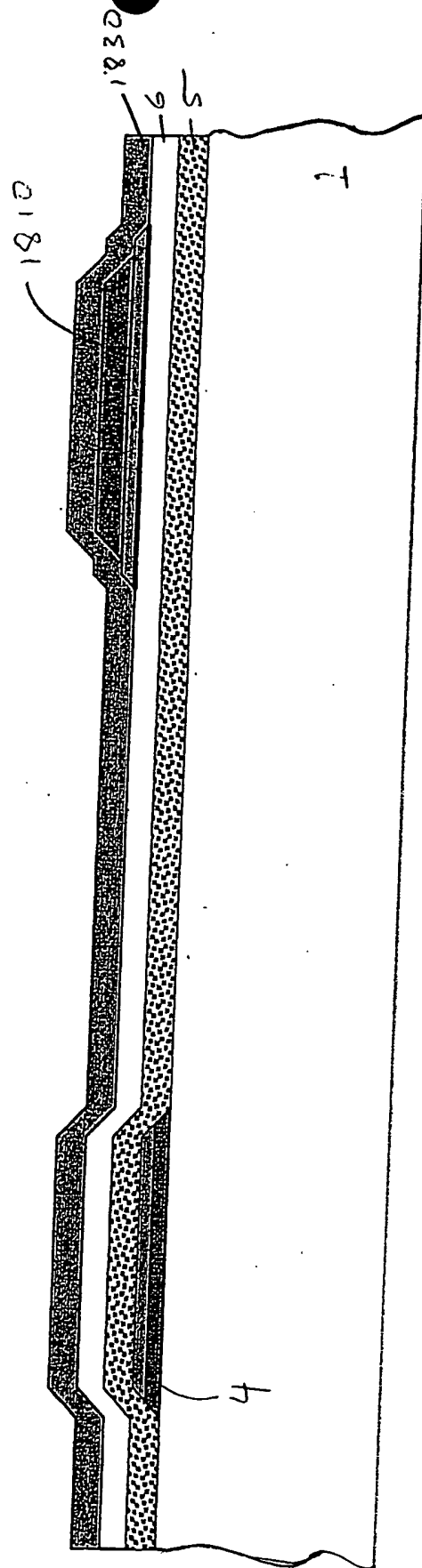


FIG. 20H

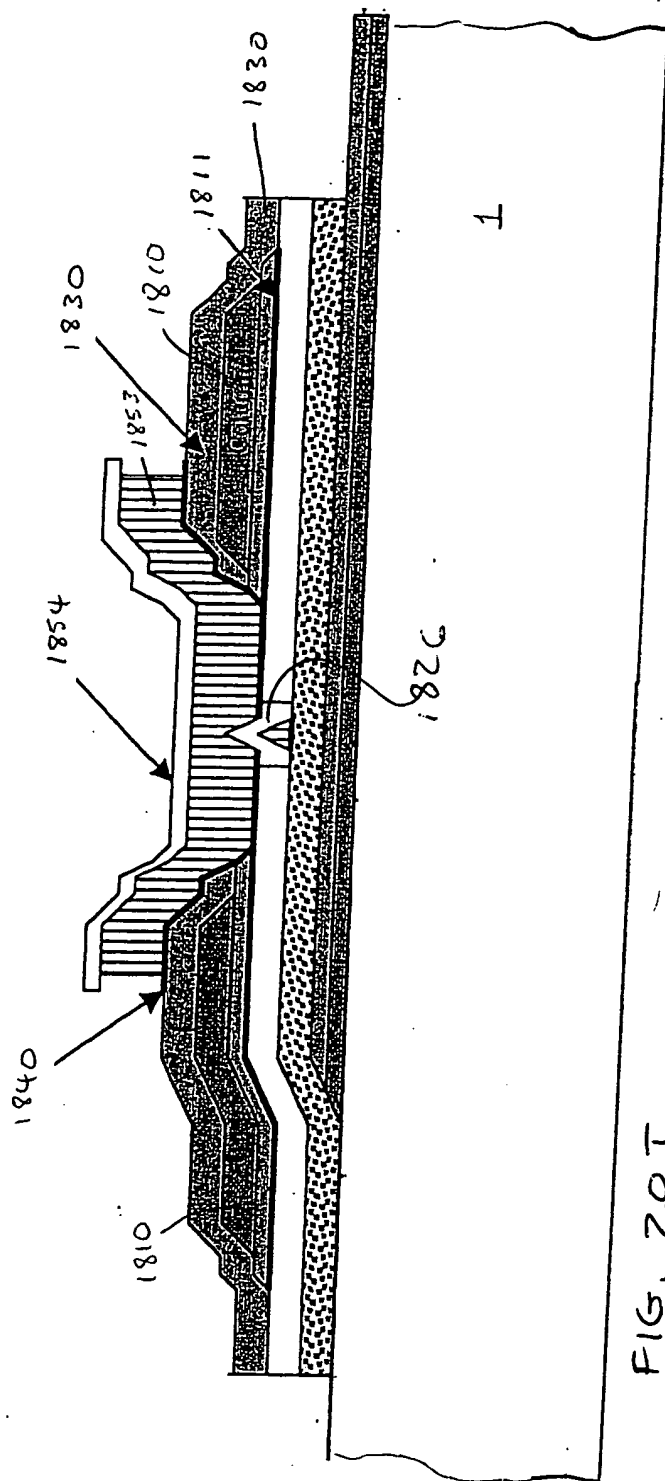


FIG. 20I

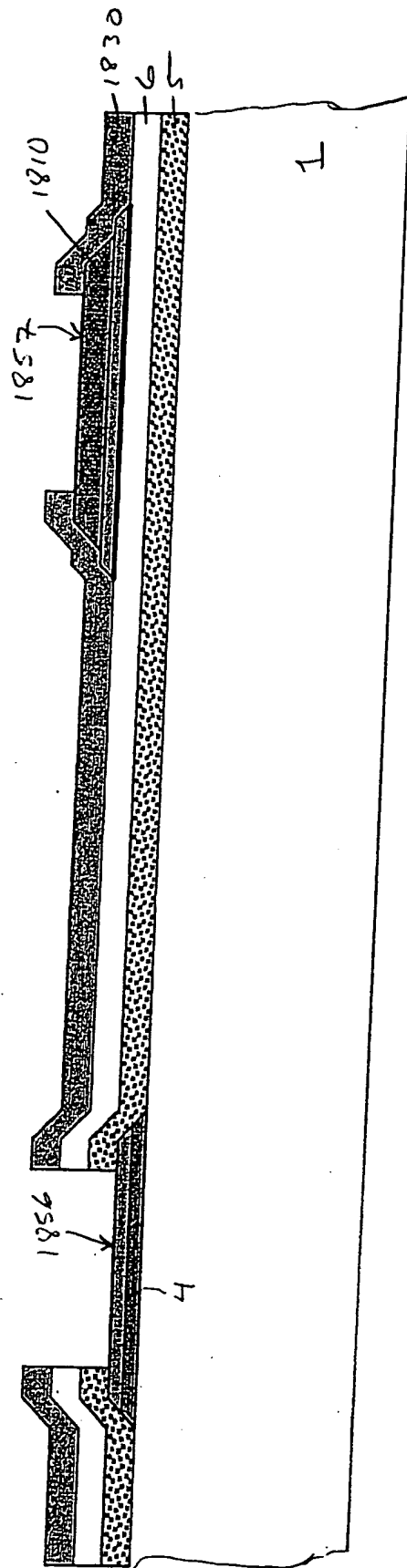
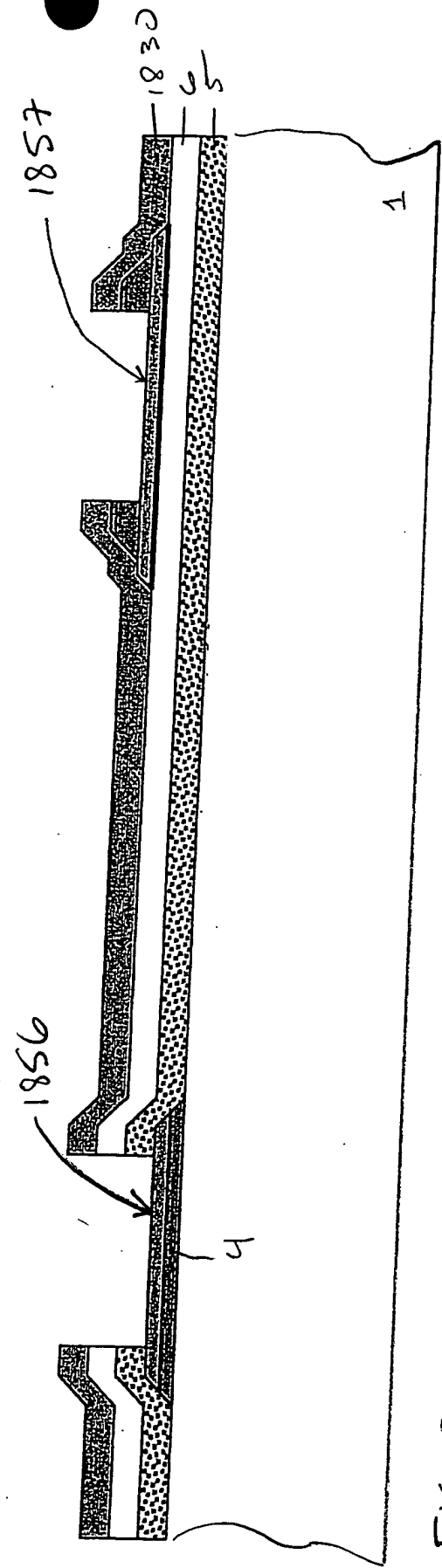
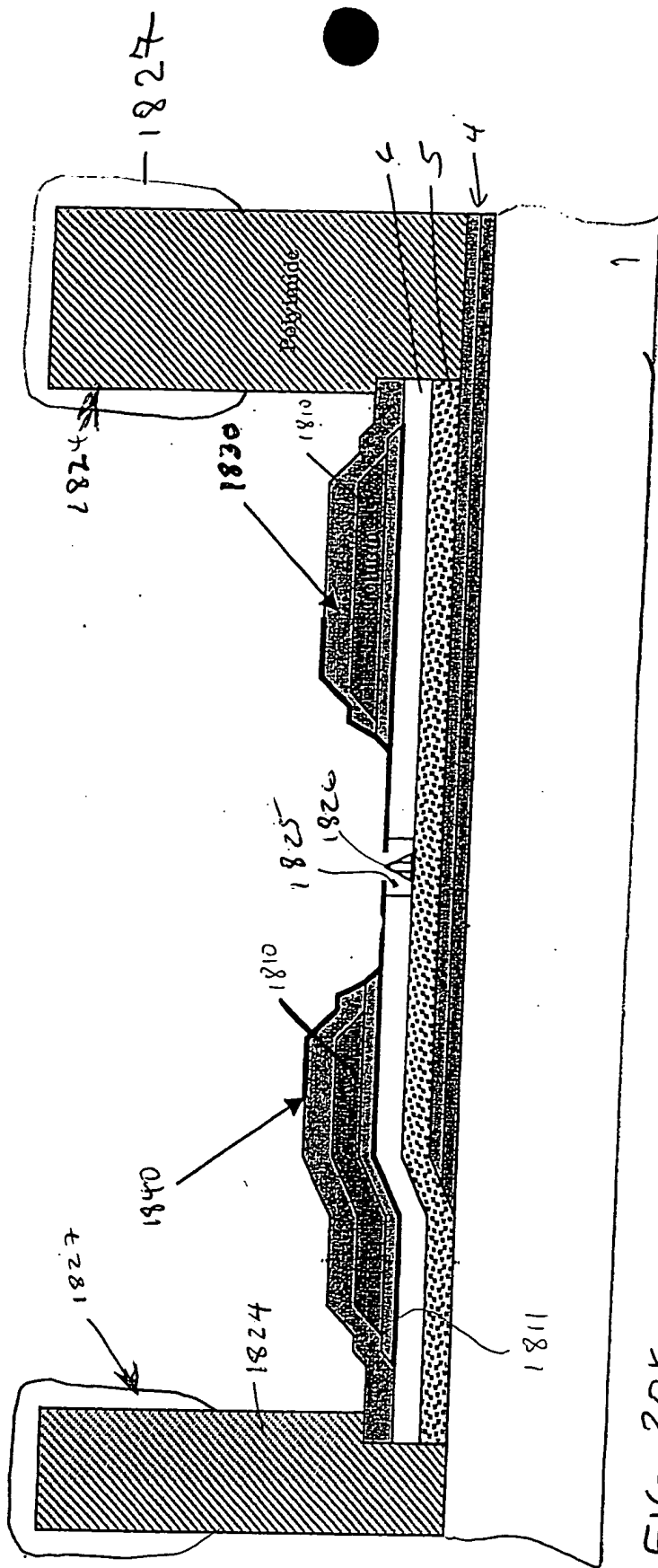


FIG. 20J



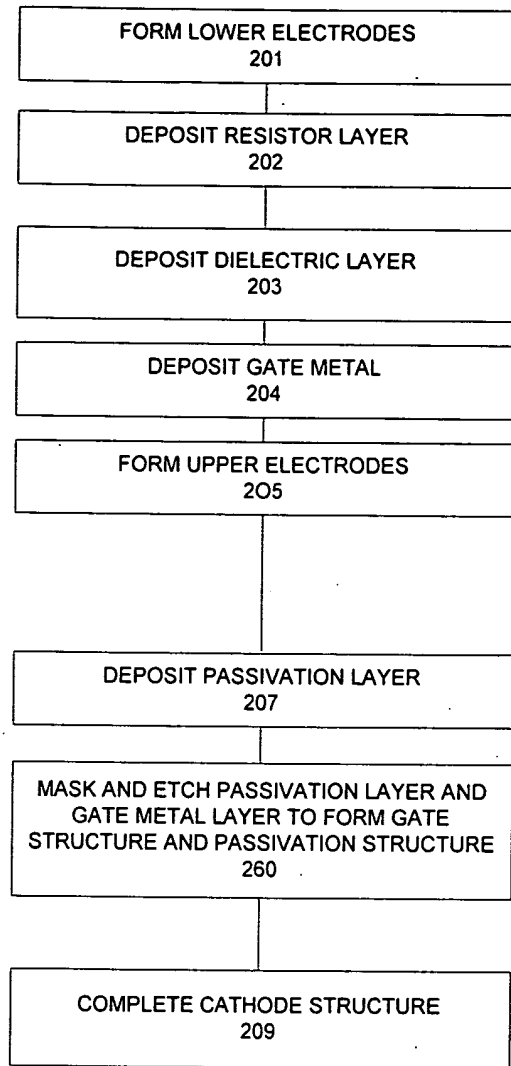


FIG. 21

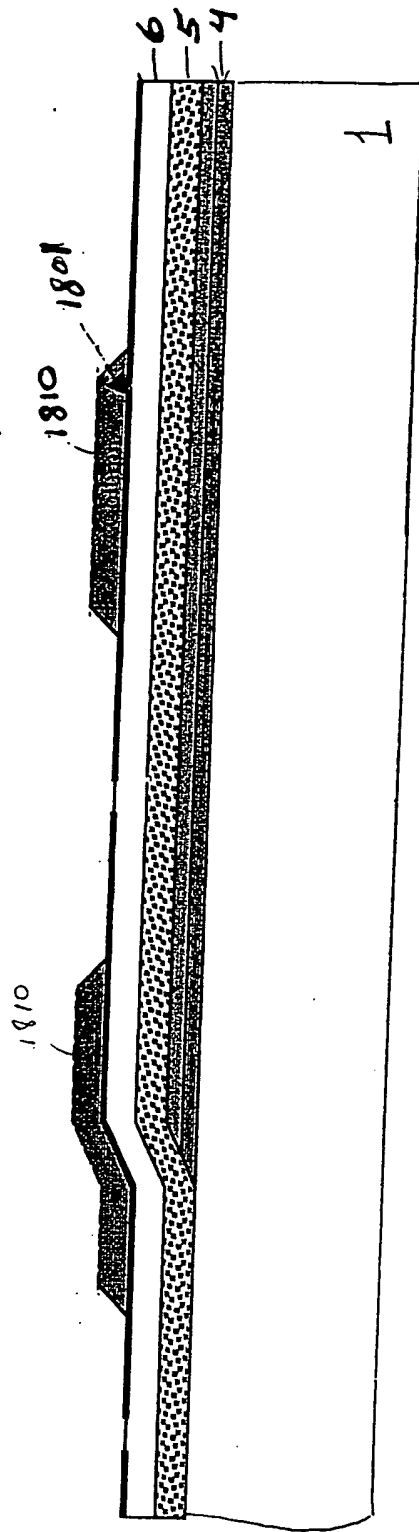


FIG. 22A

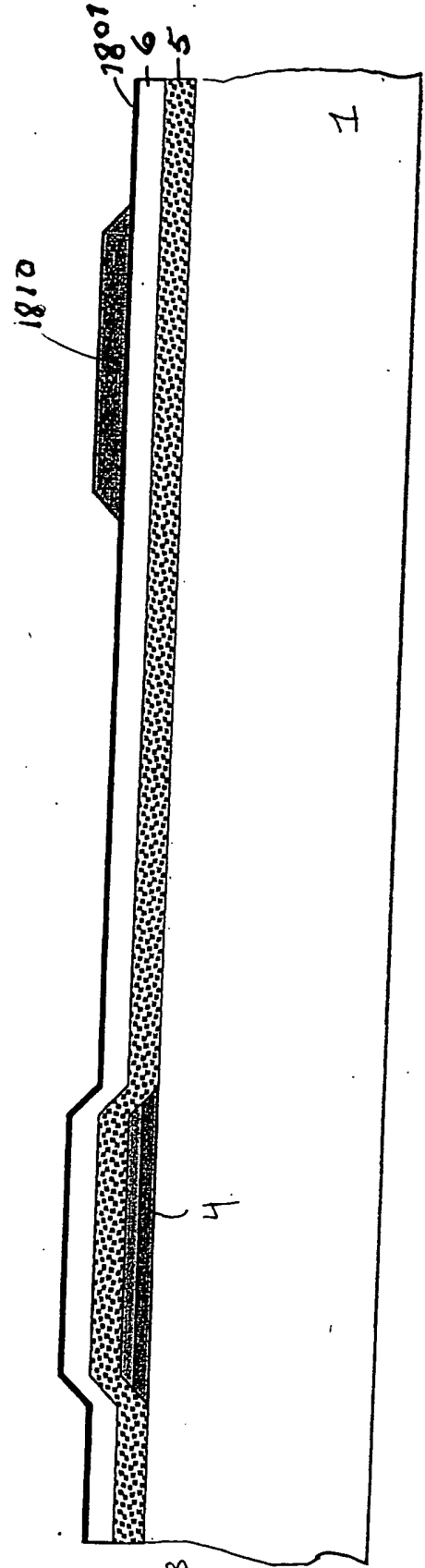


FIG. 22B

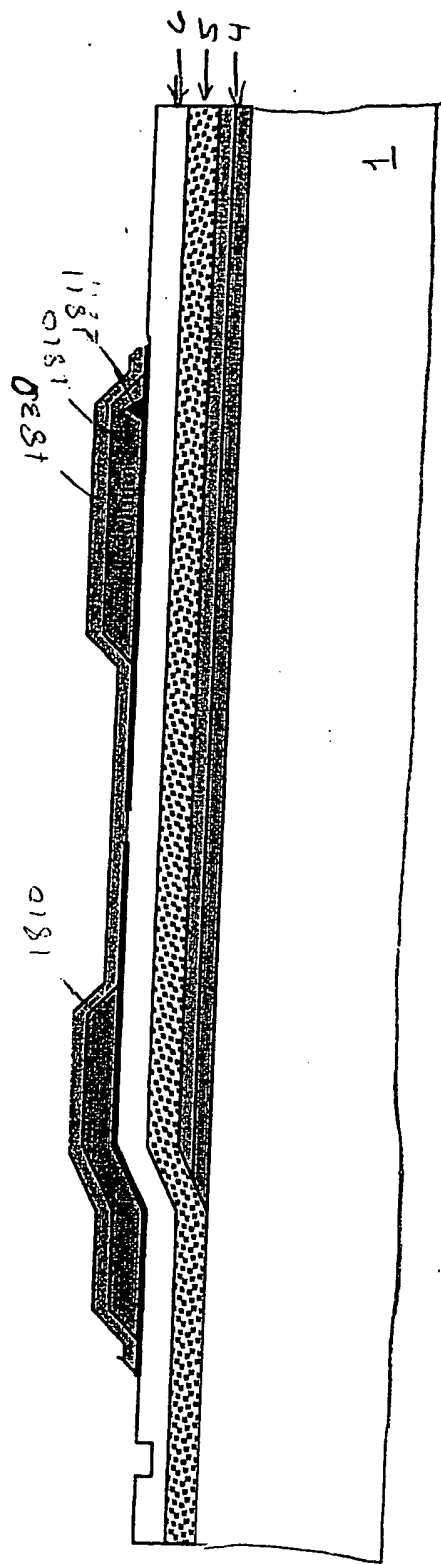


FIG. 22C

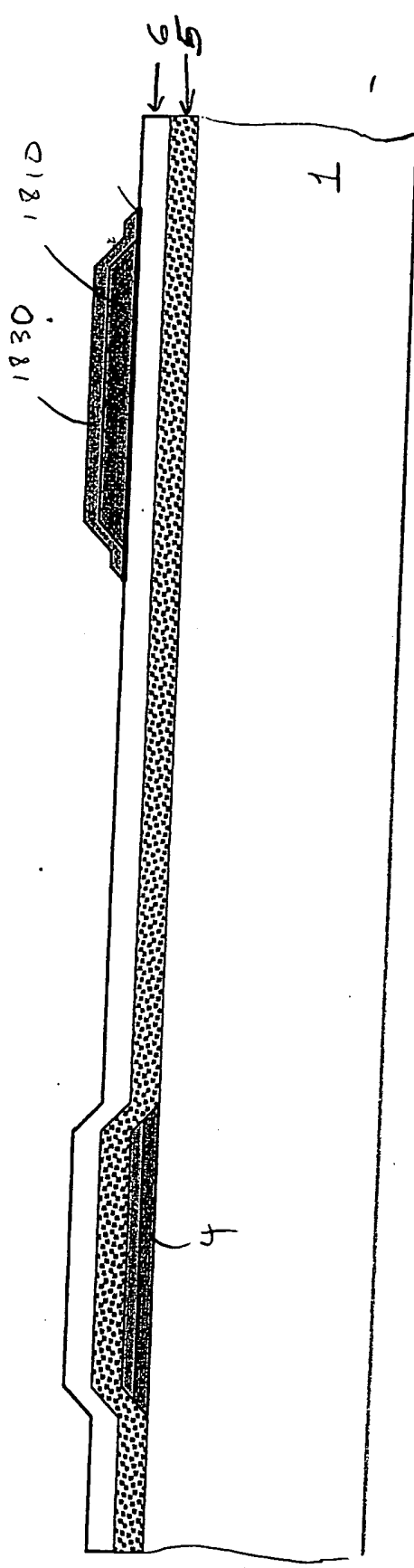
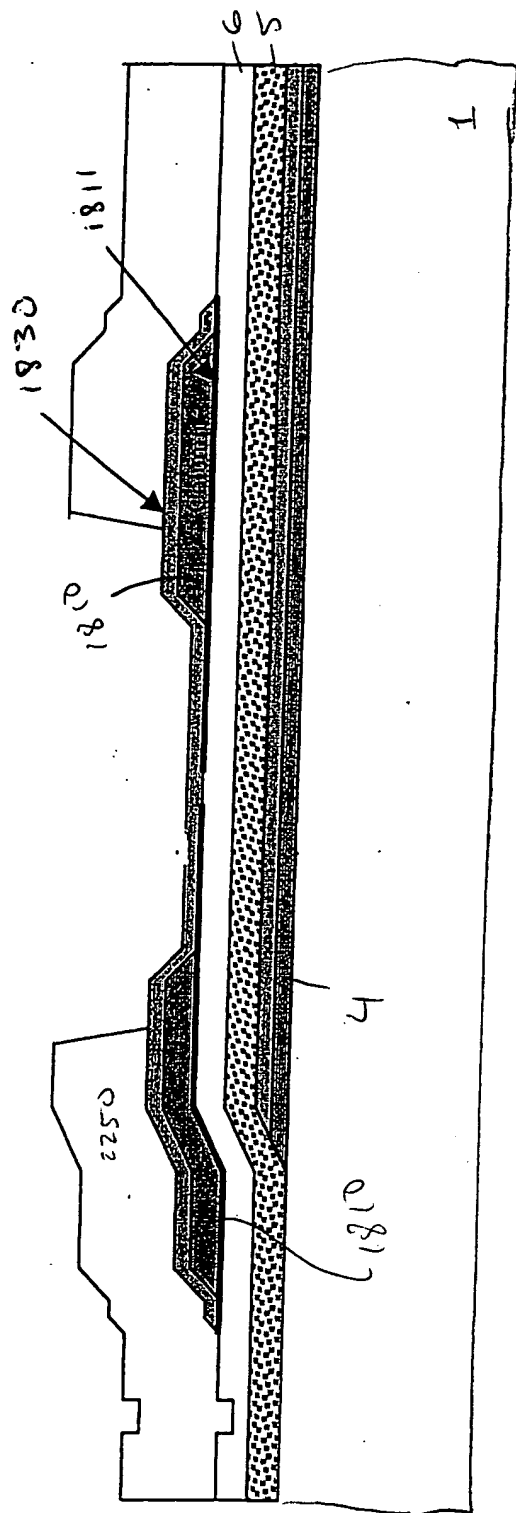
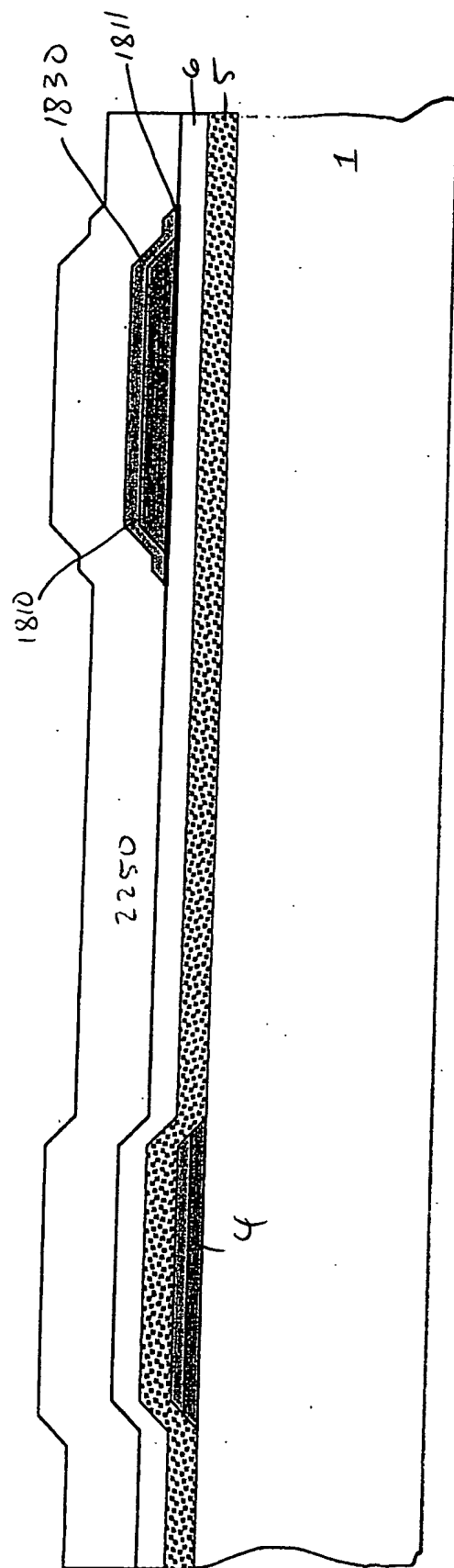


FIG. 22D



F1622E



322917

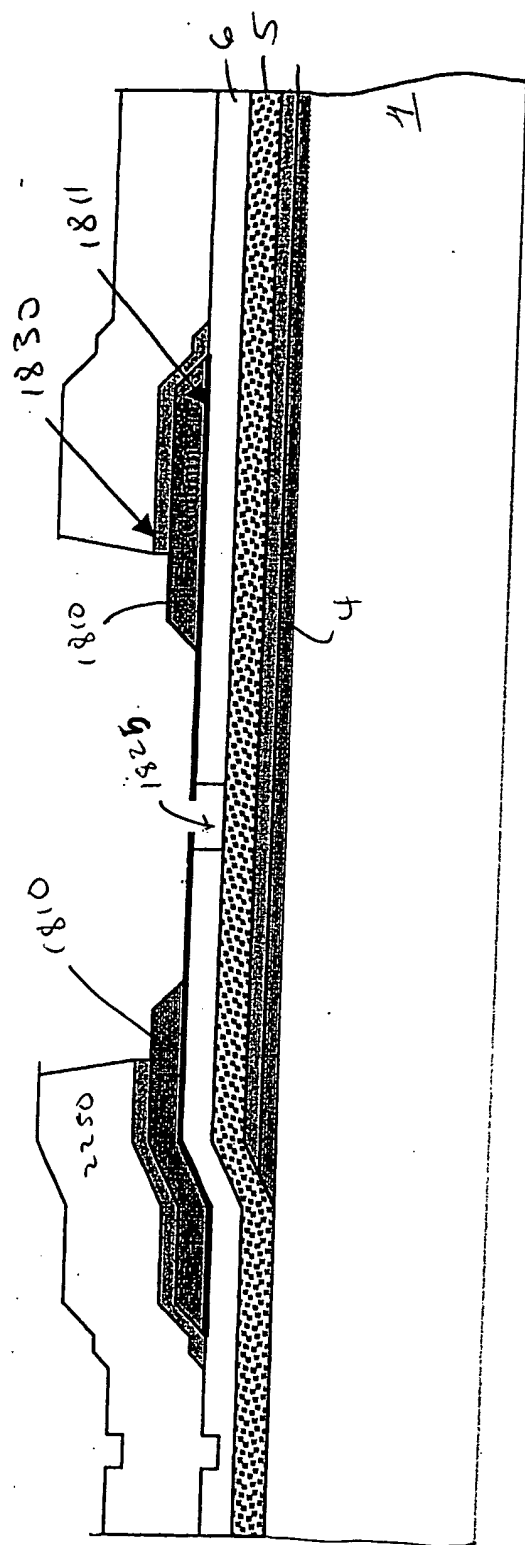
[illegible]

FIG 22G

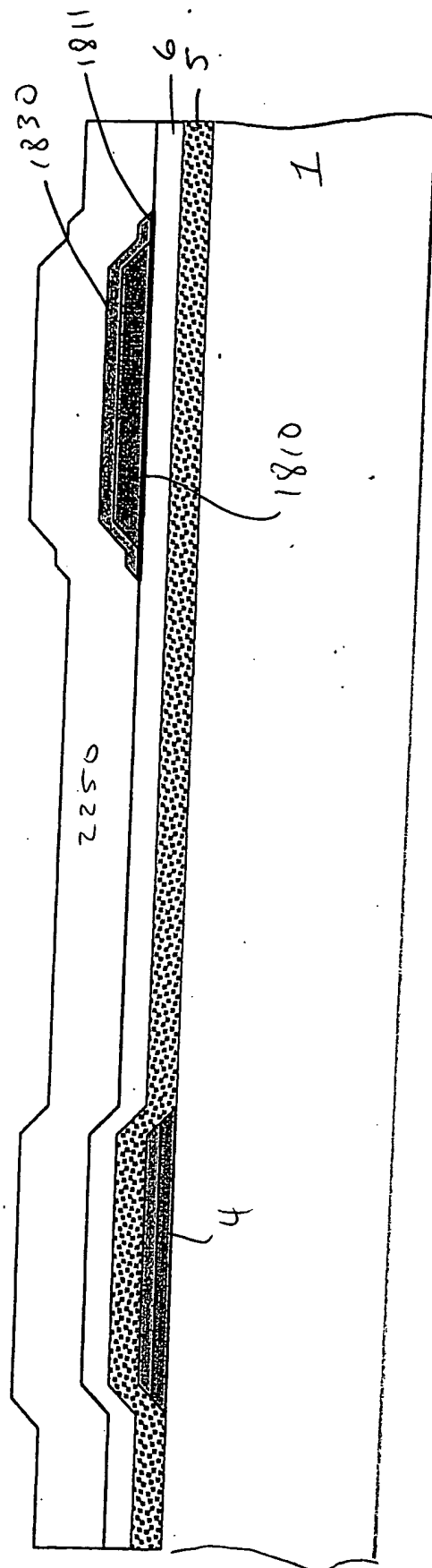


Fig 22H

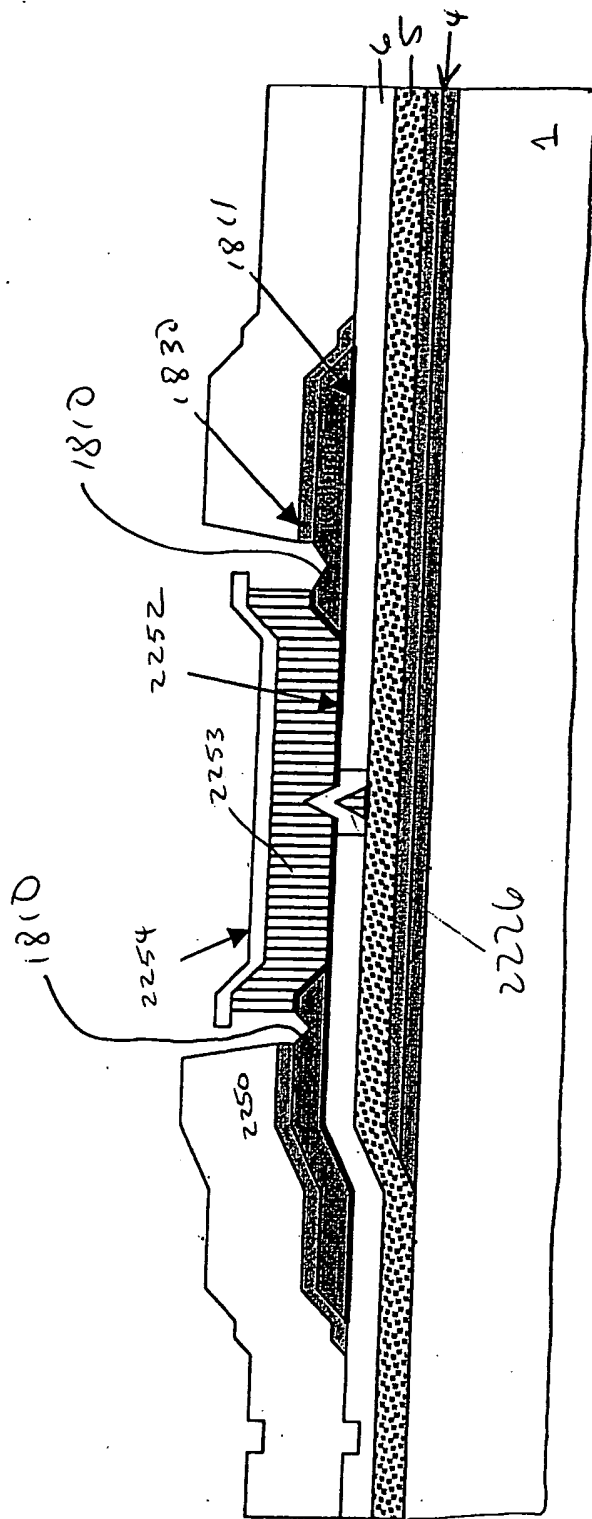


FIG. 22I

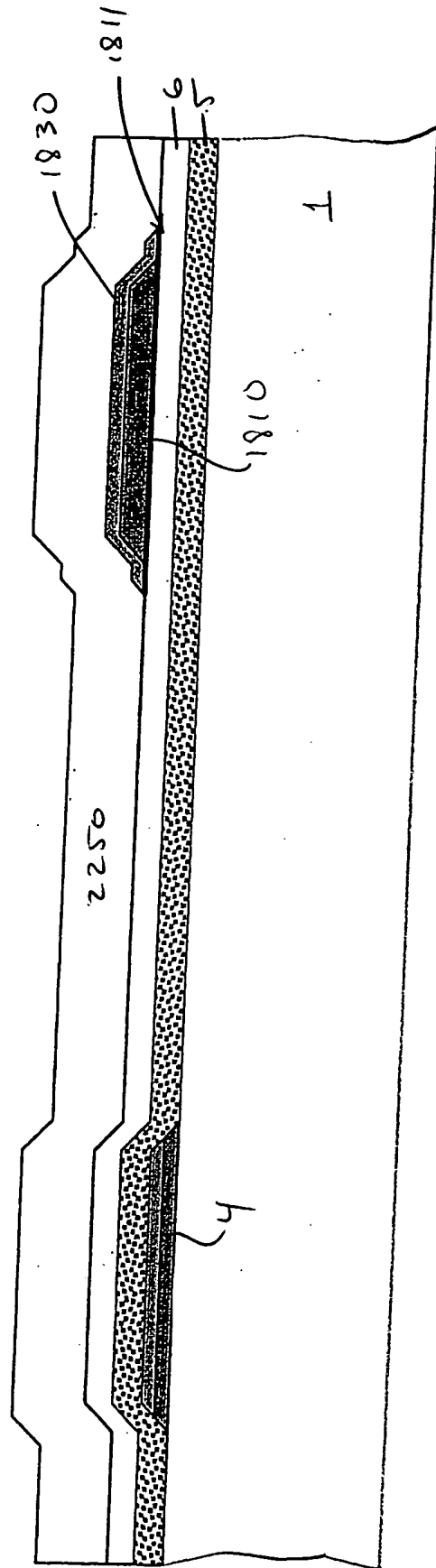
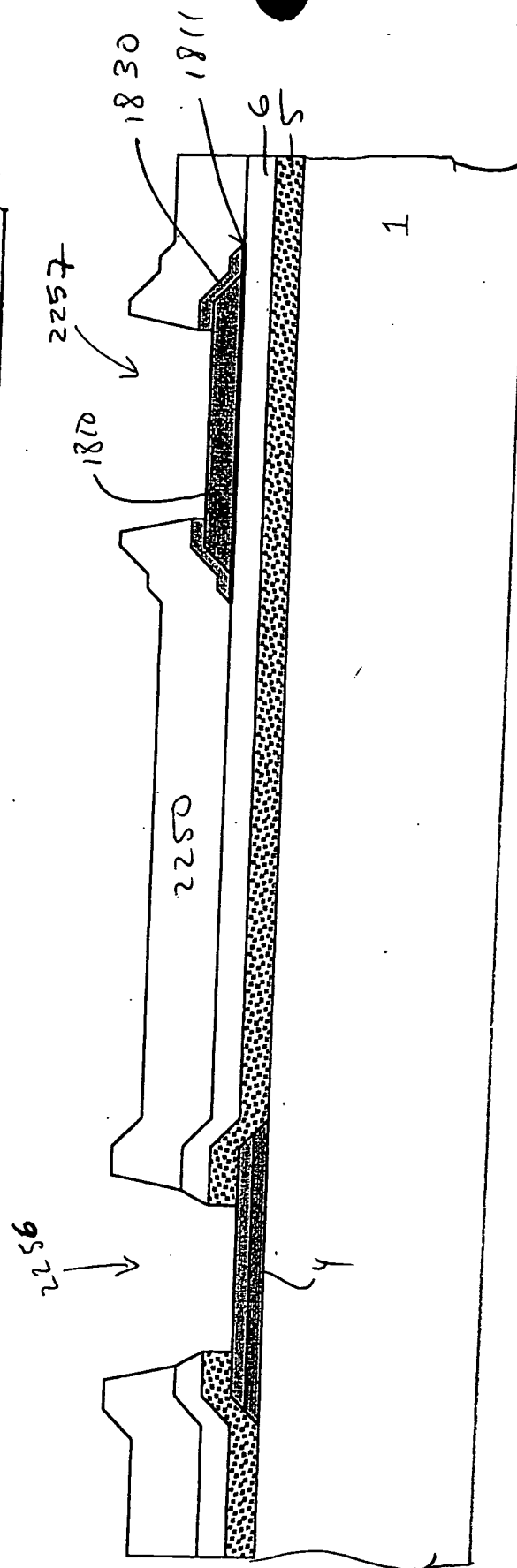
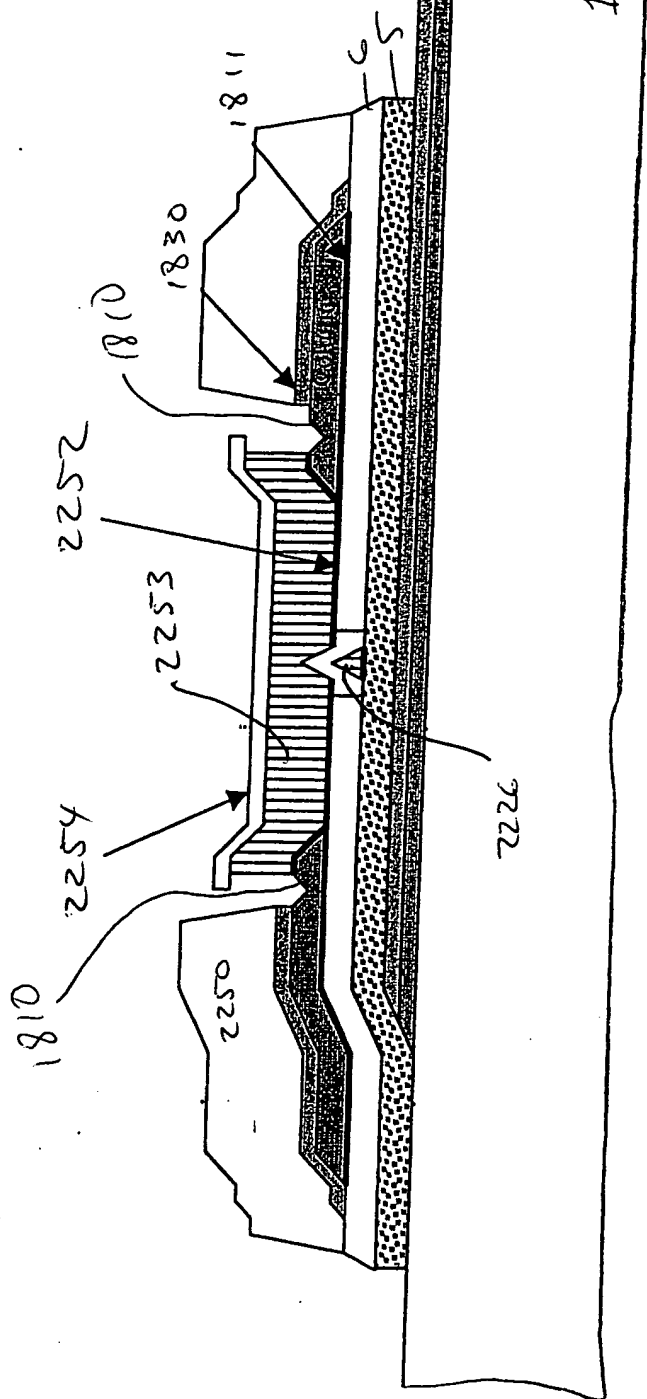
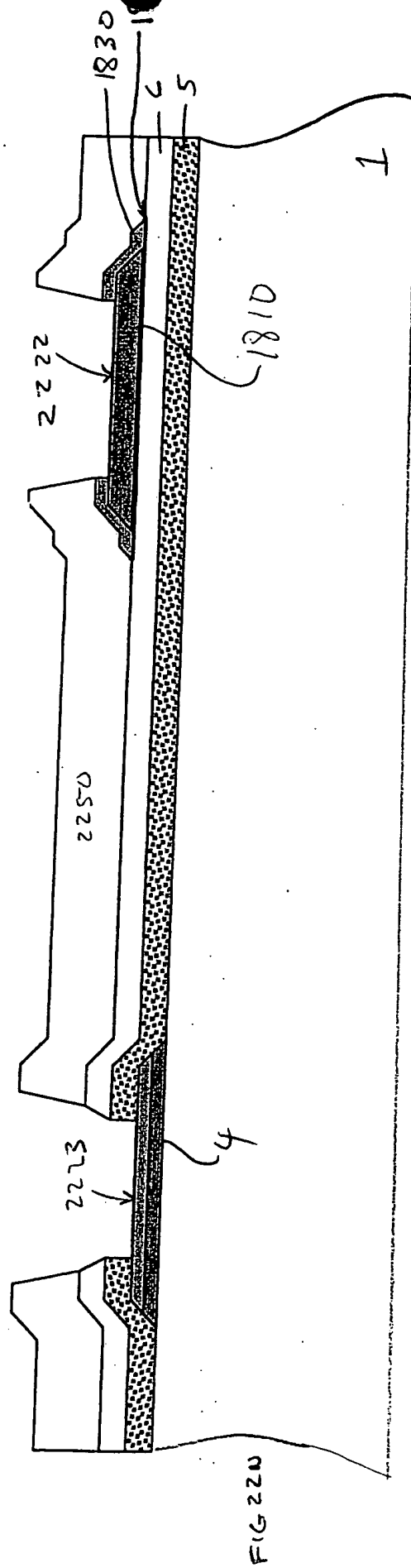
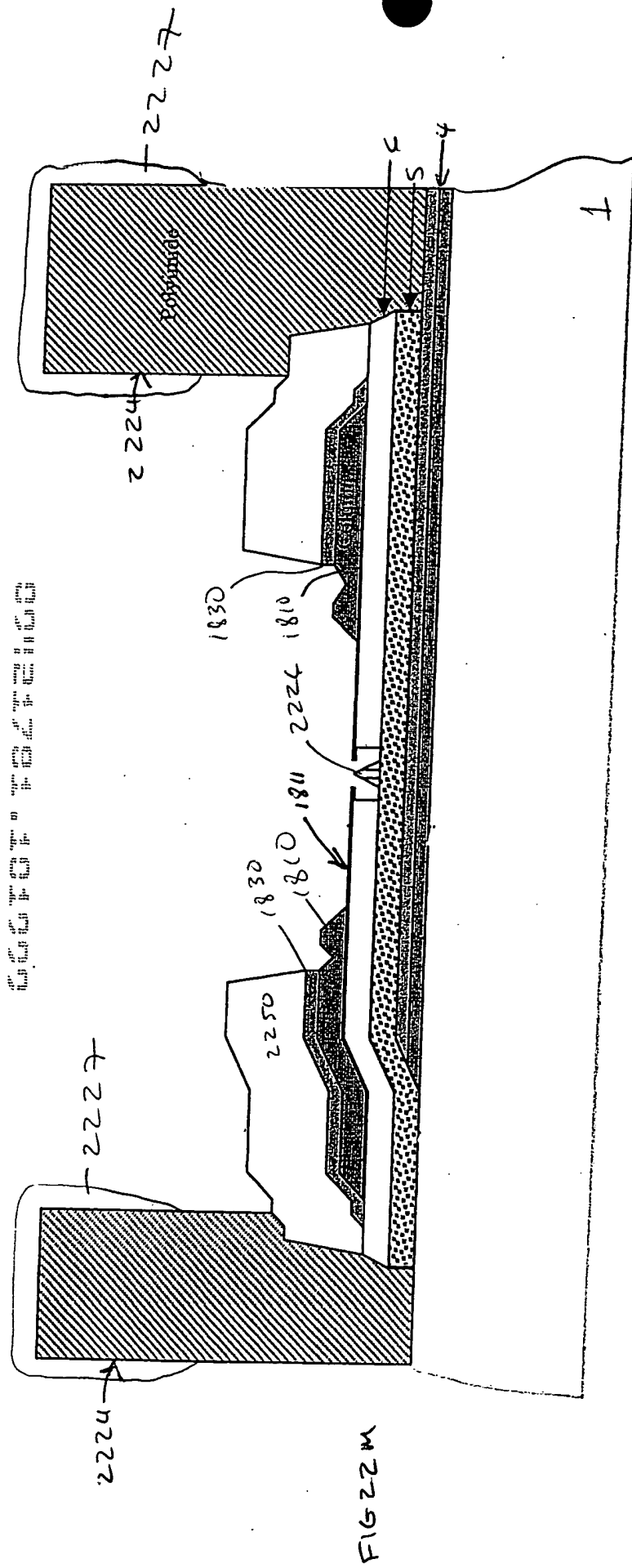


FIG. 22J





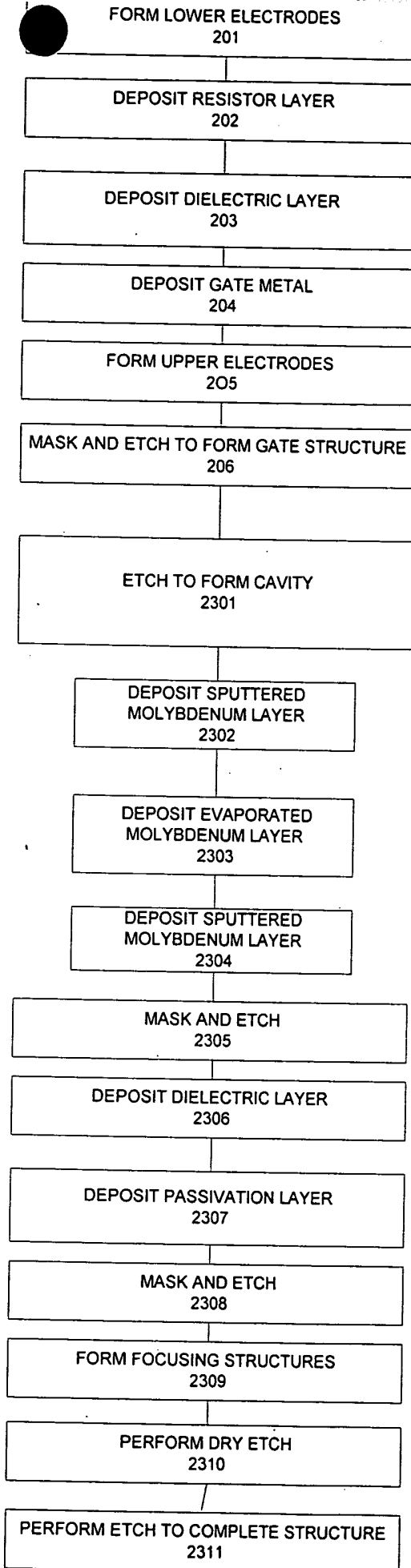


FIG. 23

U.S. Pat. No. 4,811,000

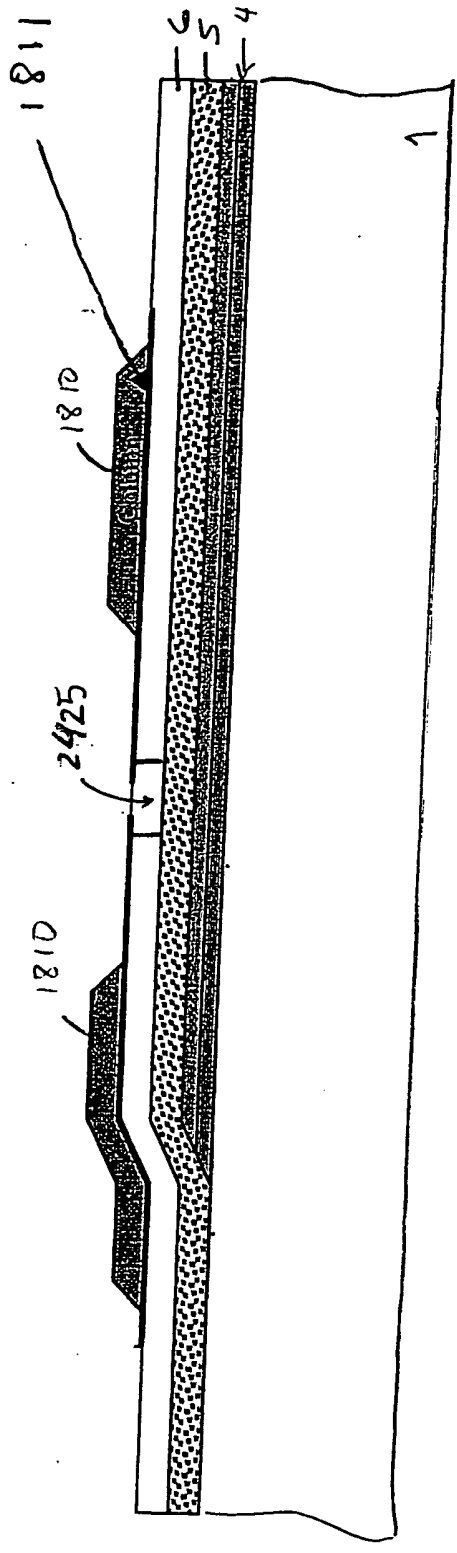


FIG 24A

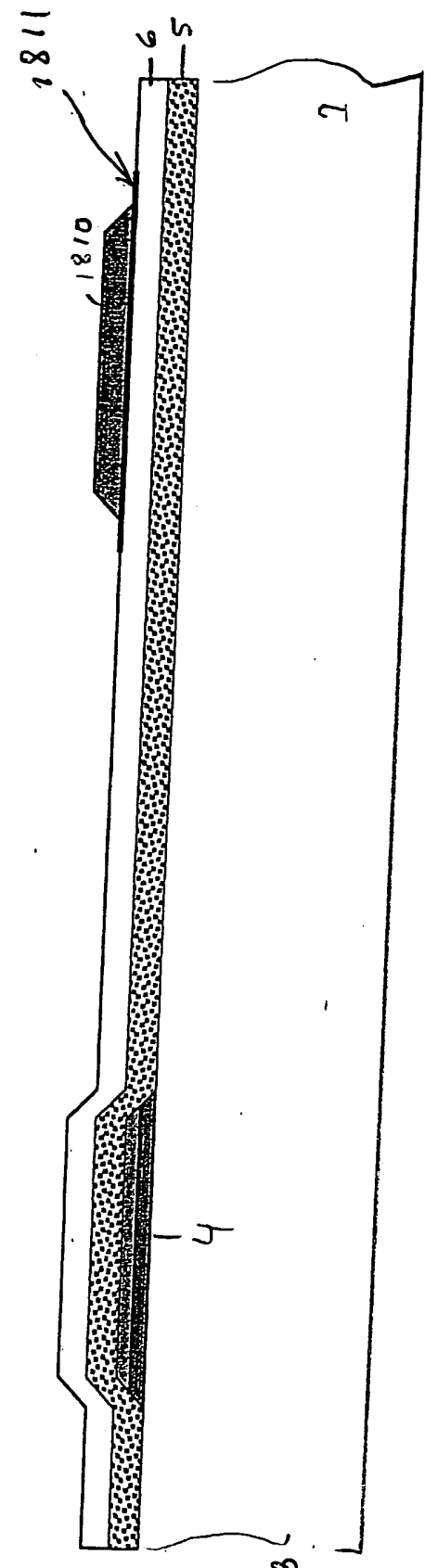


FIG. 24B

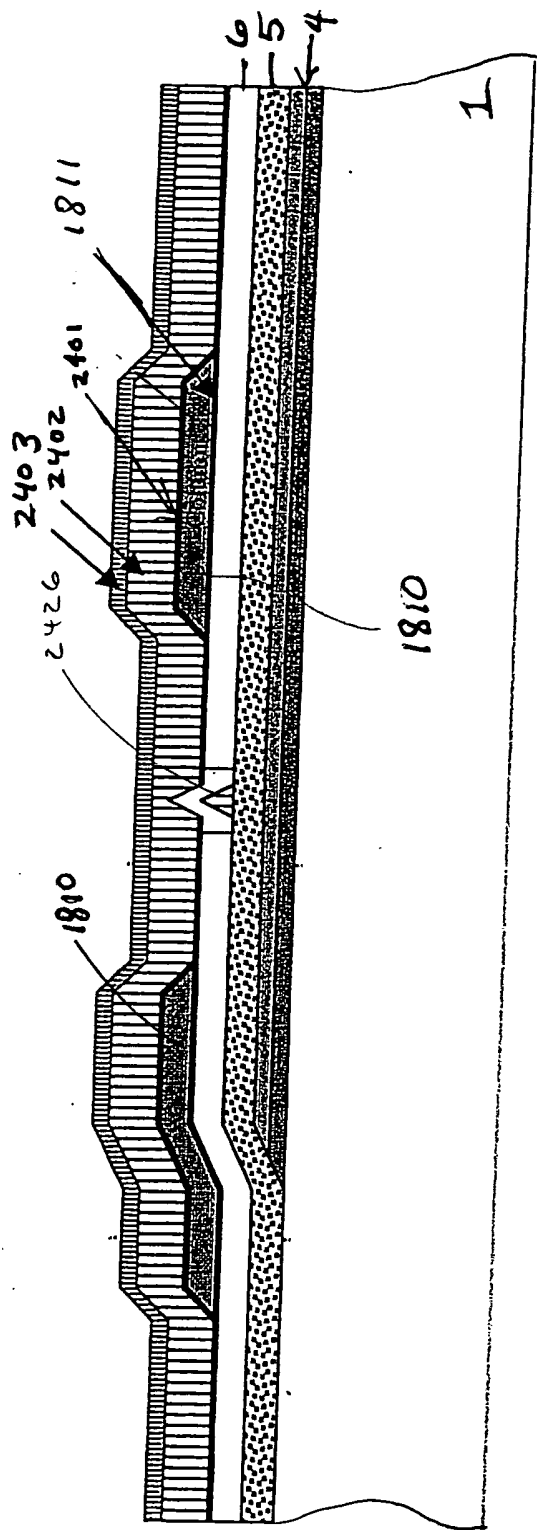


FIG 24C

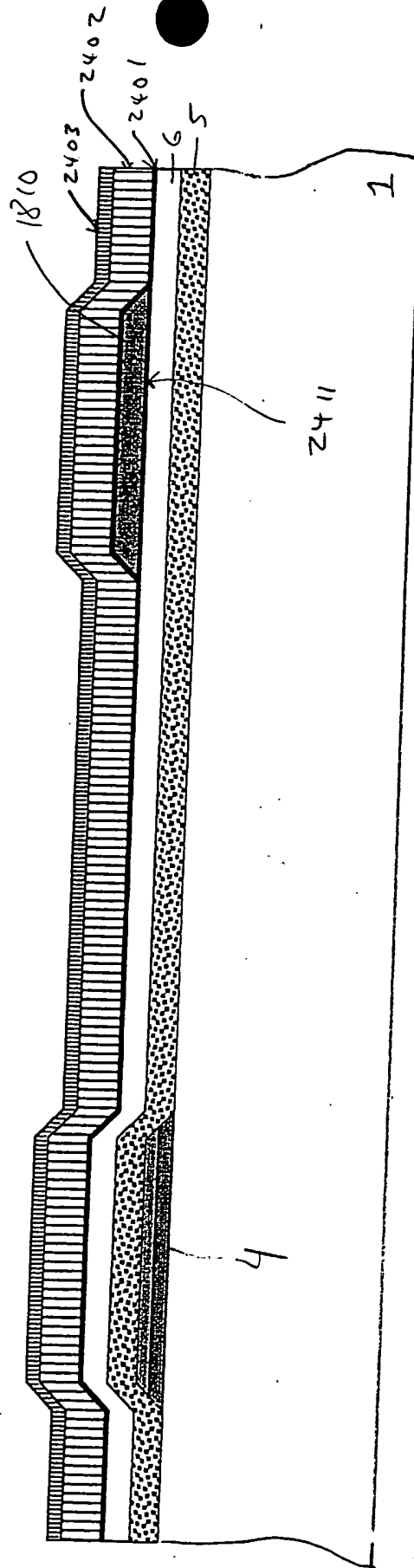
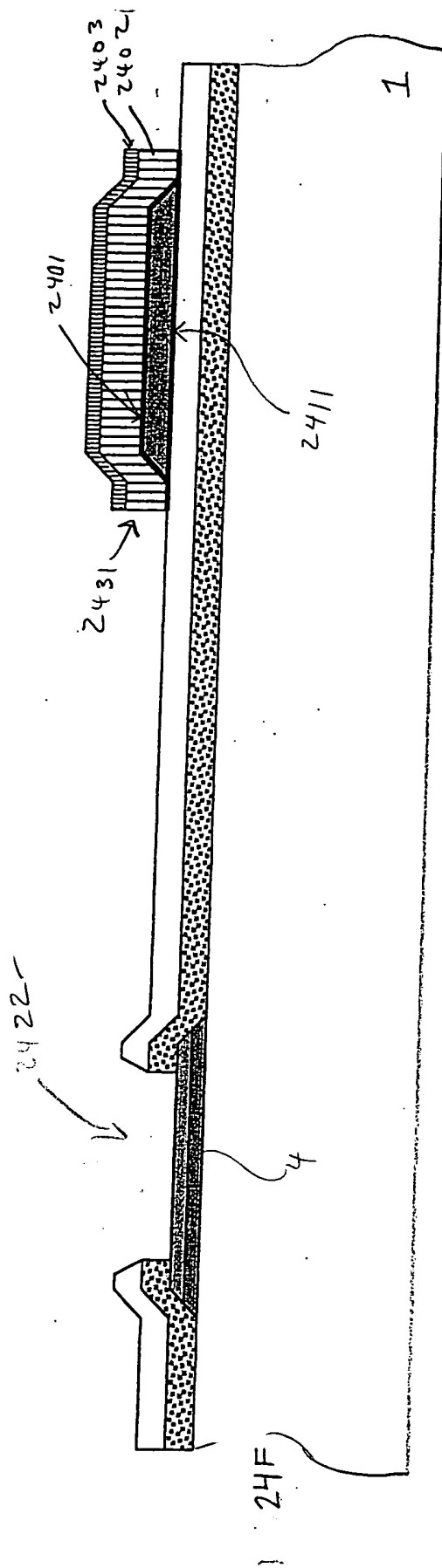
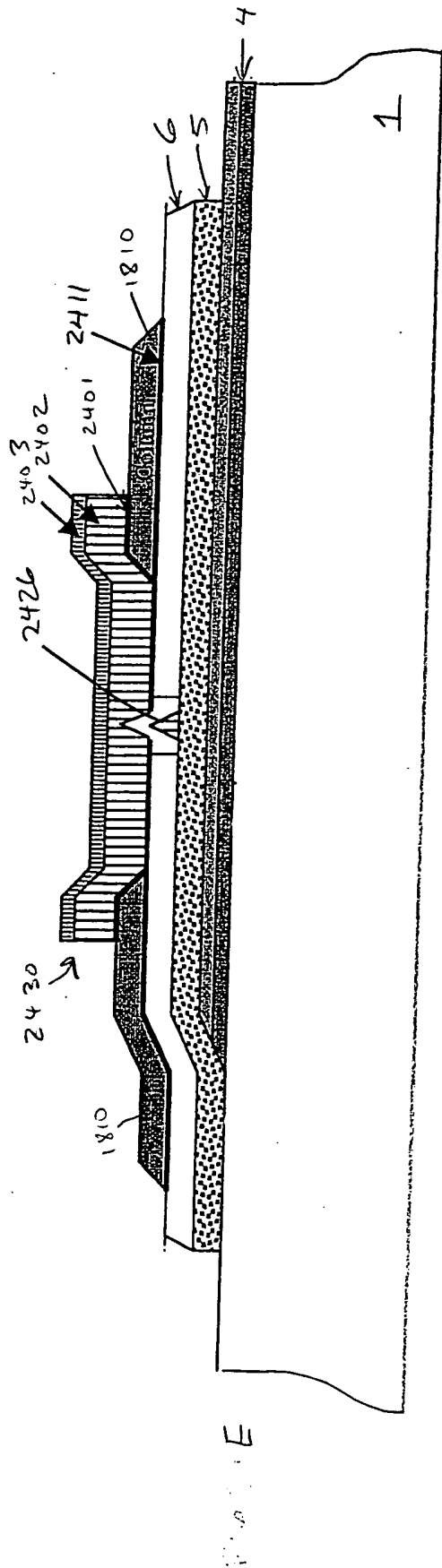


FIG 24D



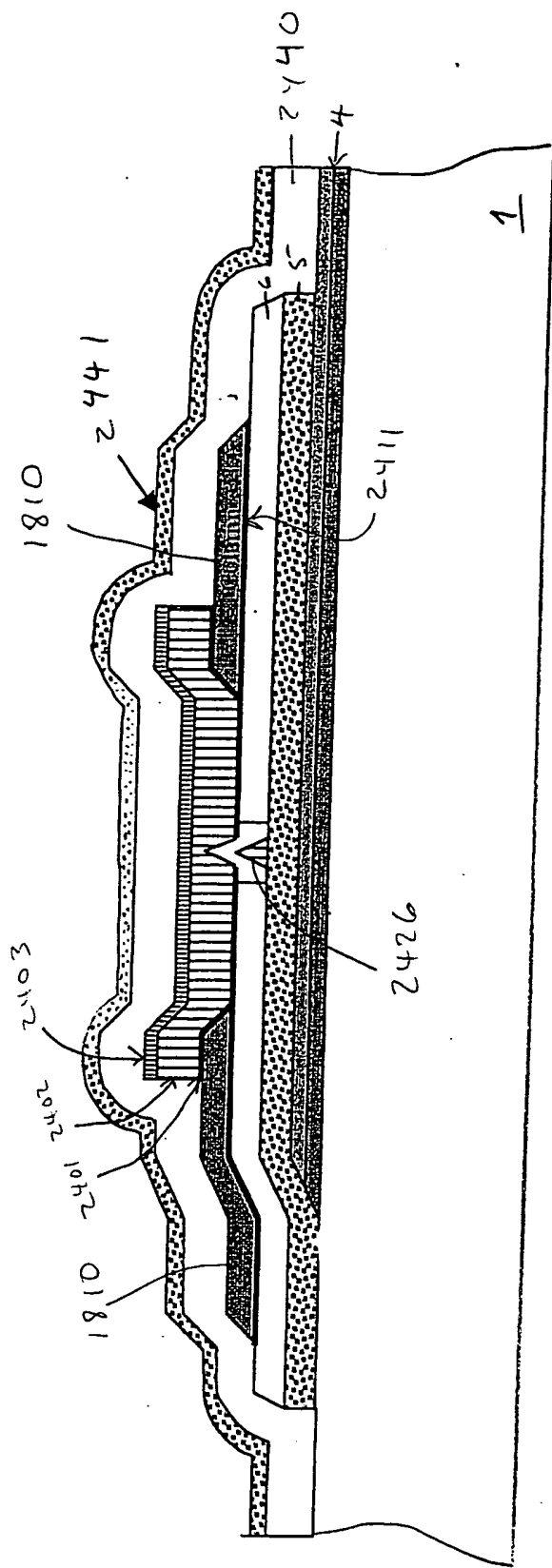
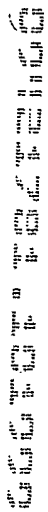
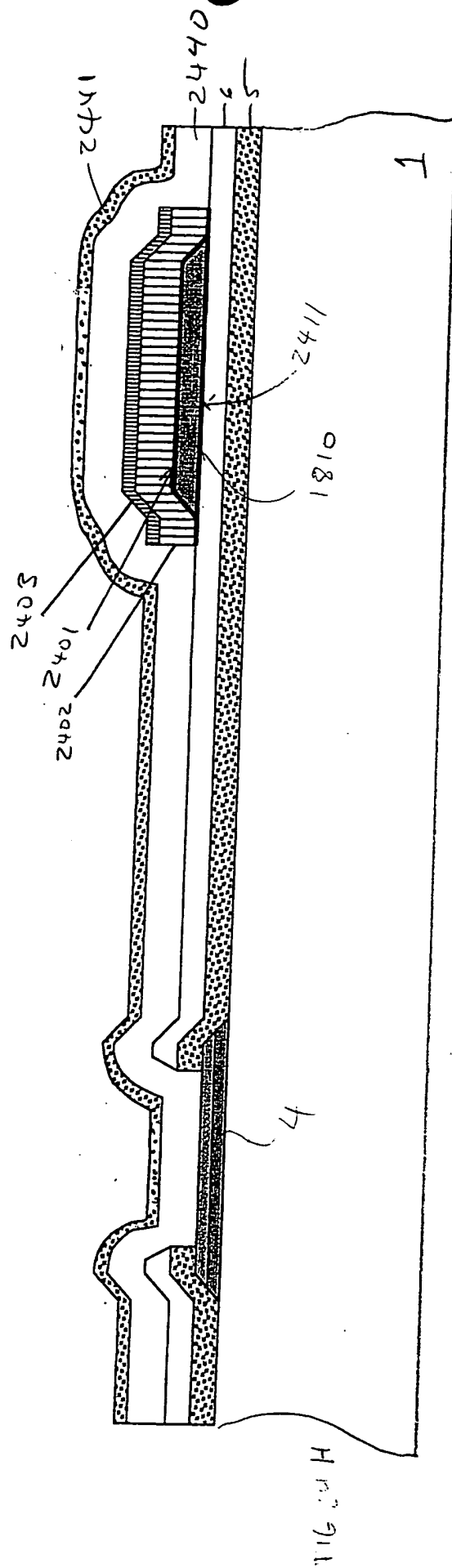
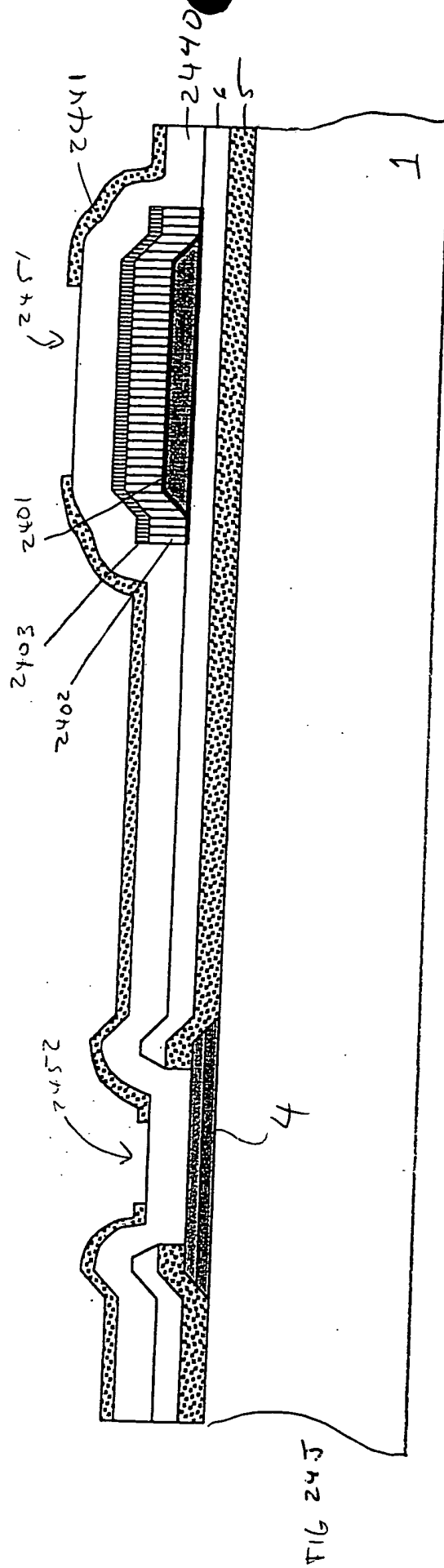
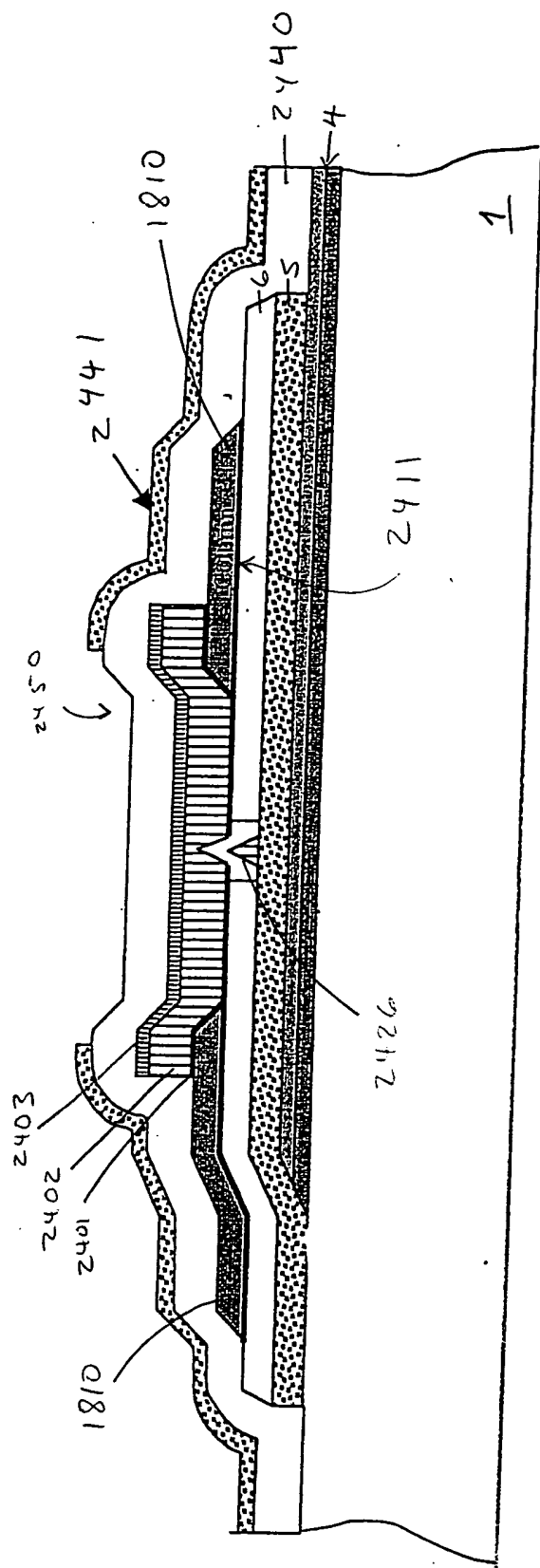


Fig. 2



Hv. 911.



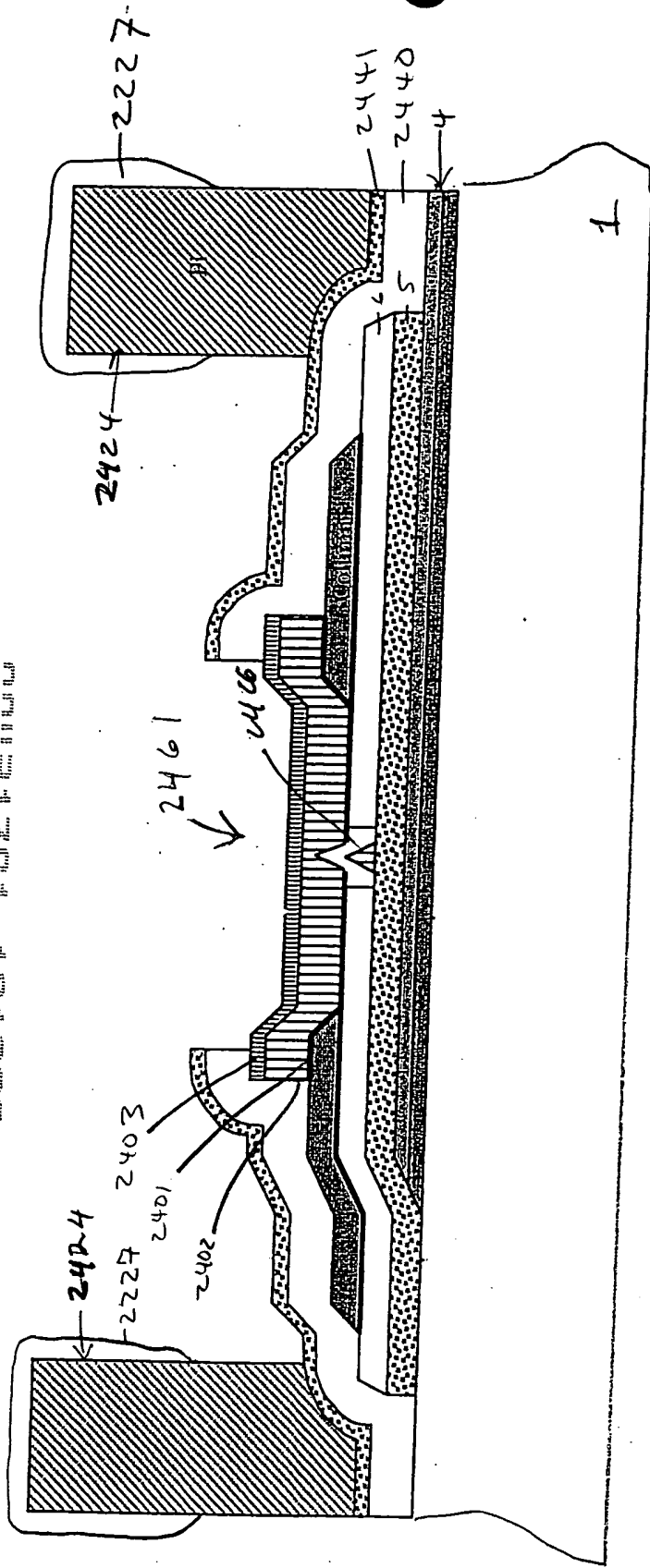


FIG 24K

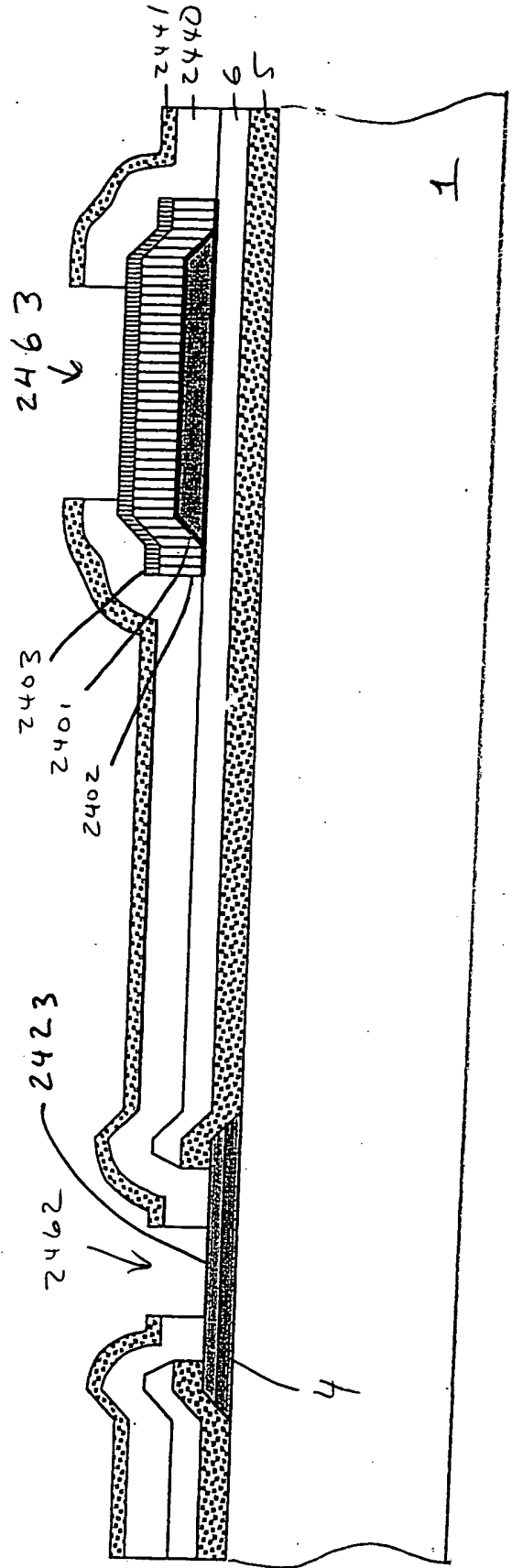


FIG 24L

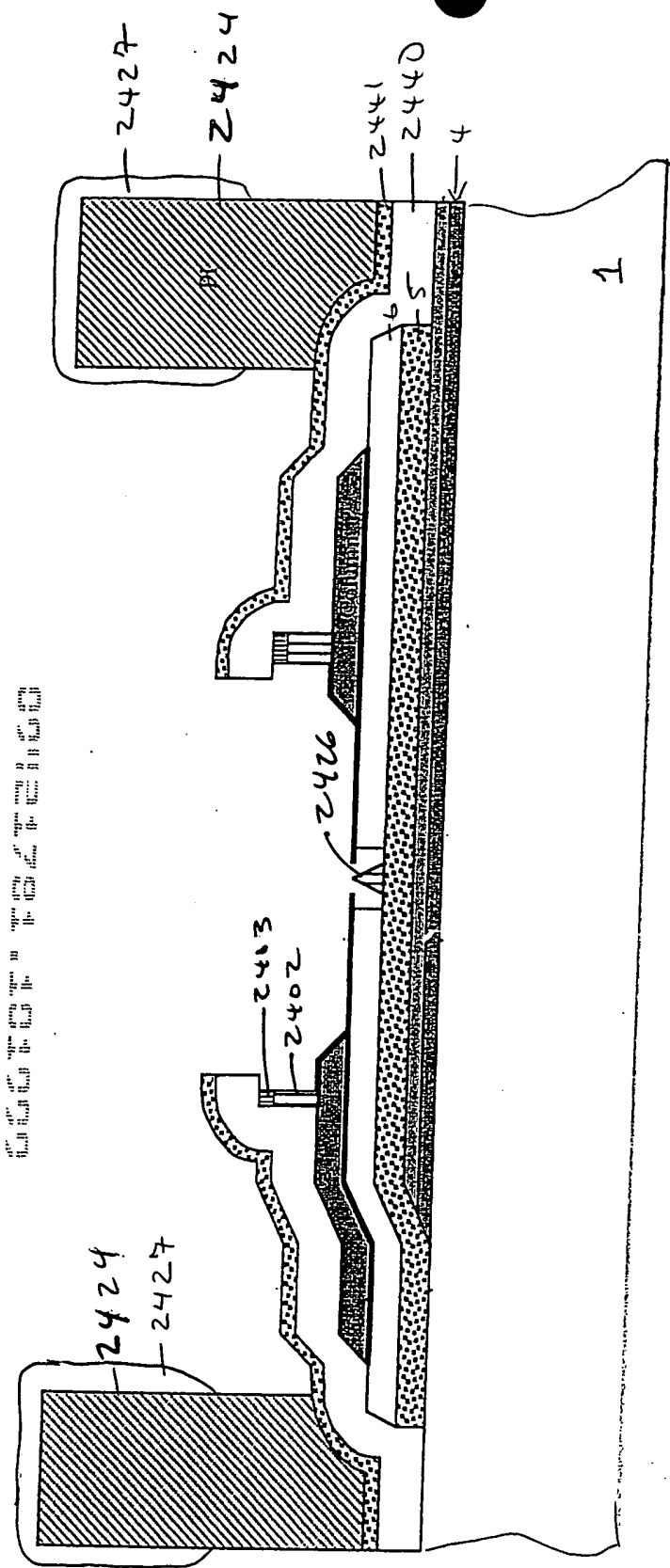


FIG. 24N

2422

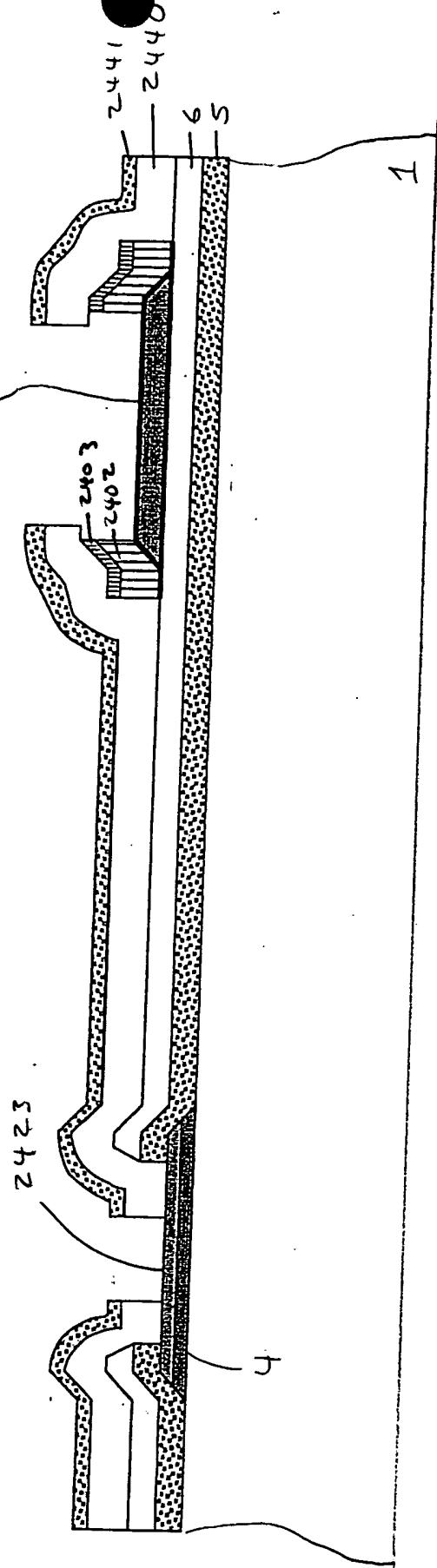
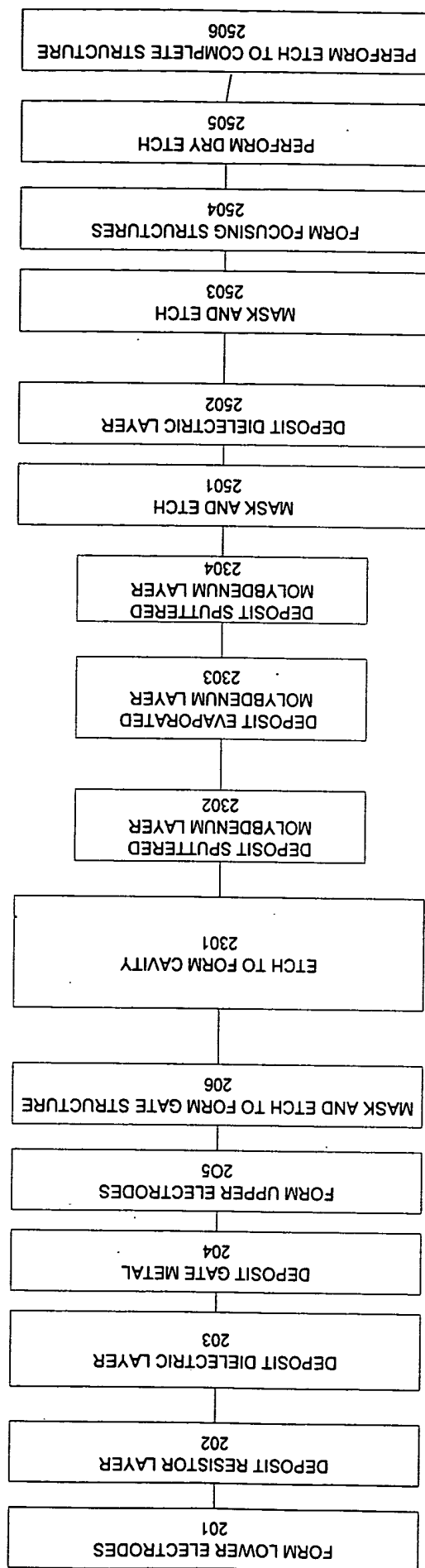


FIG. 24N

FIG. 25



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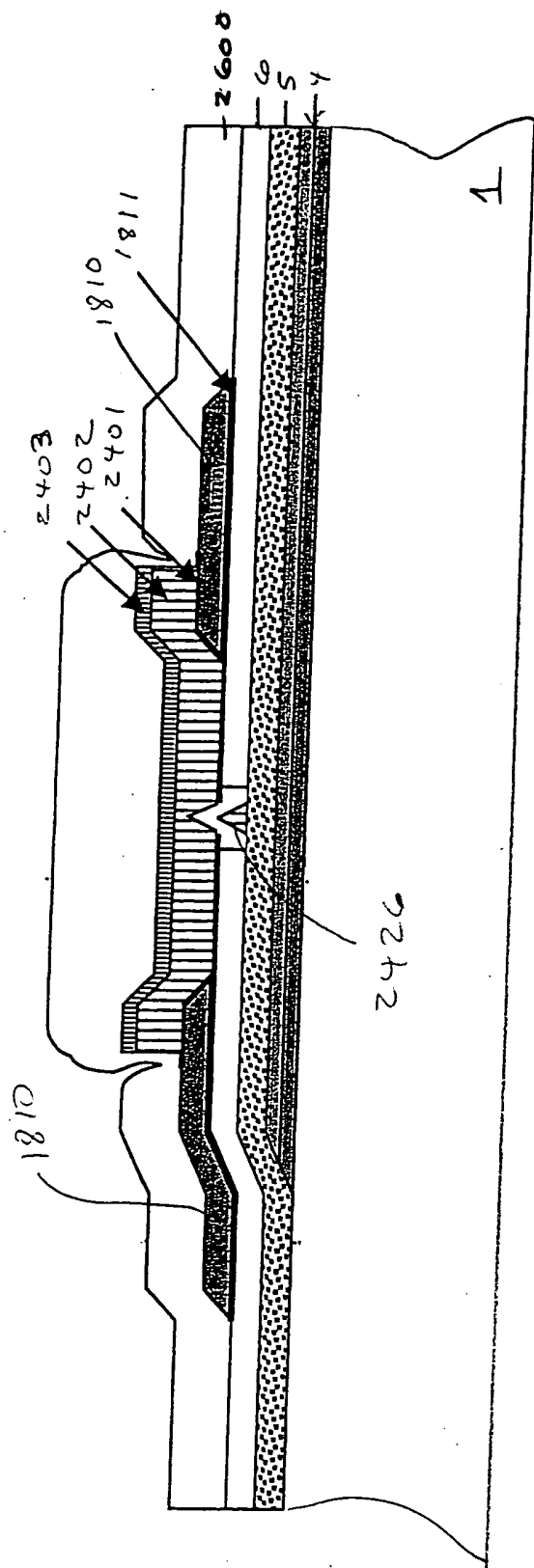
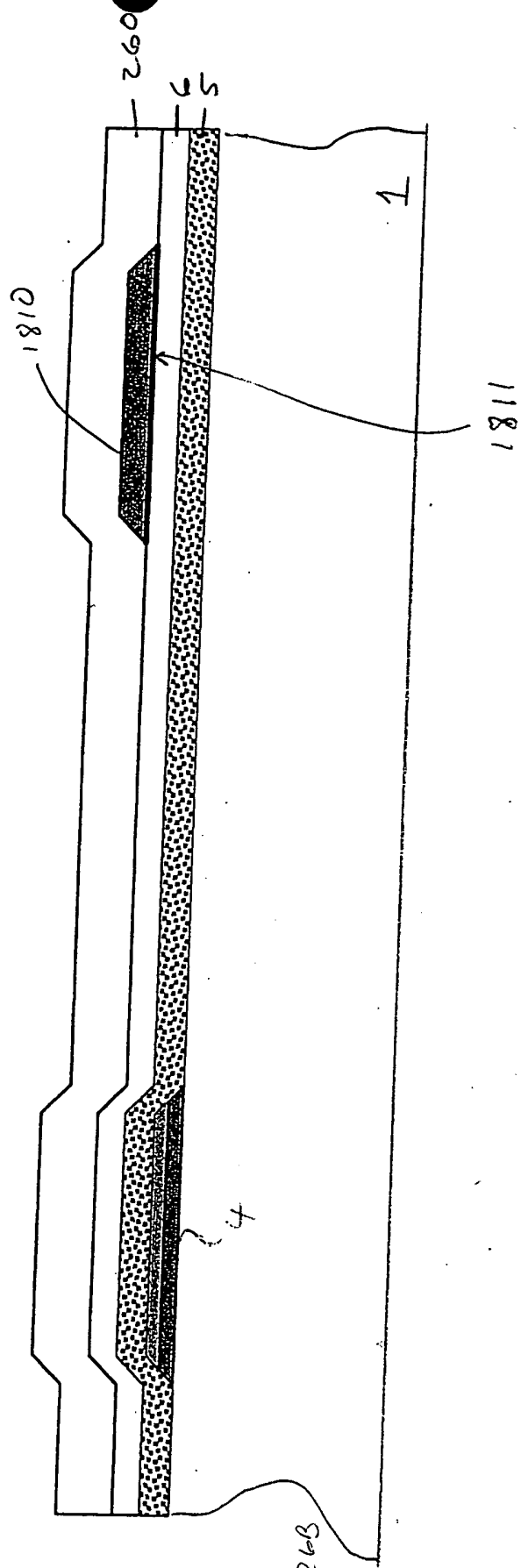


FIG. 26A



F.16.26B

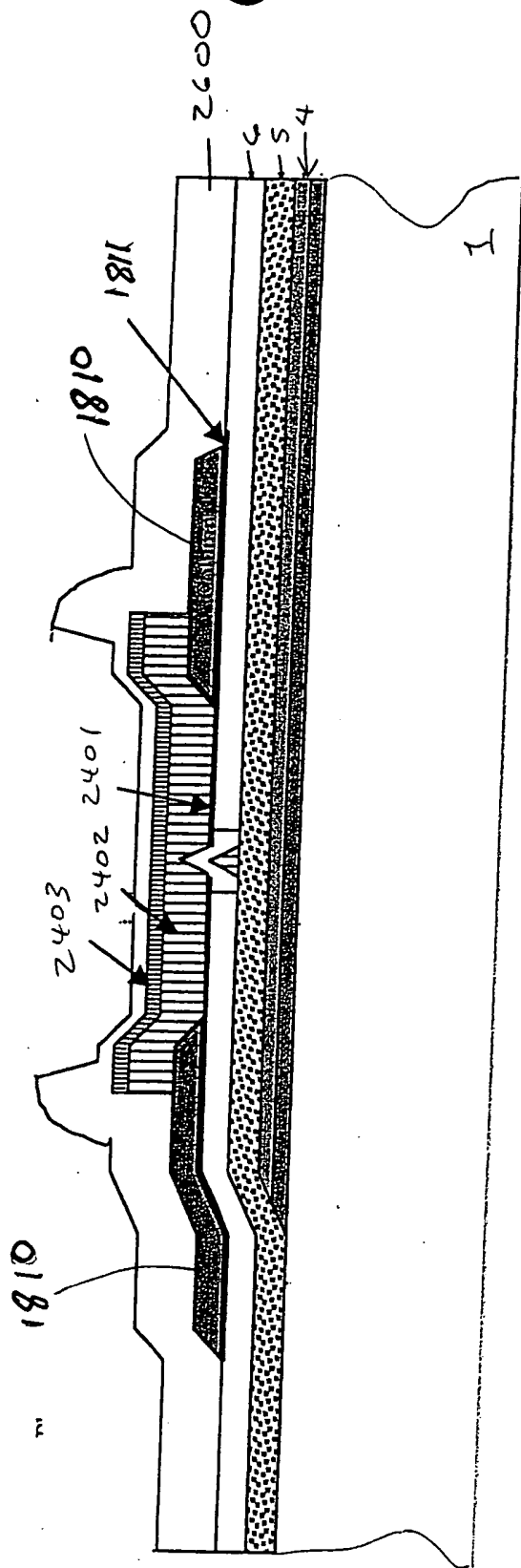


FIG 26C

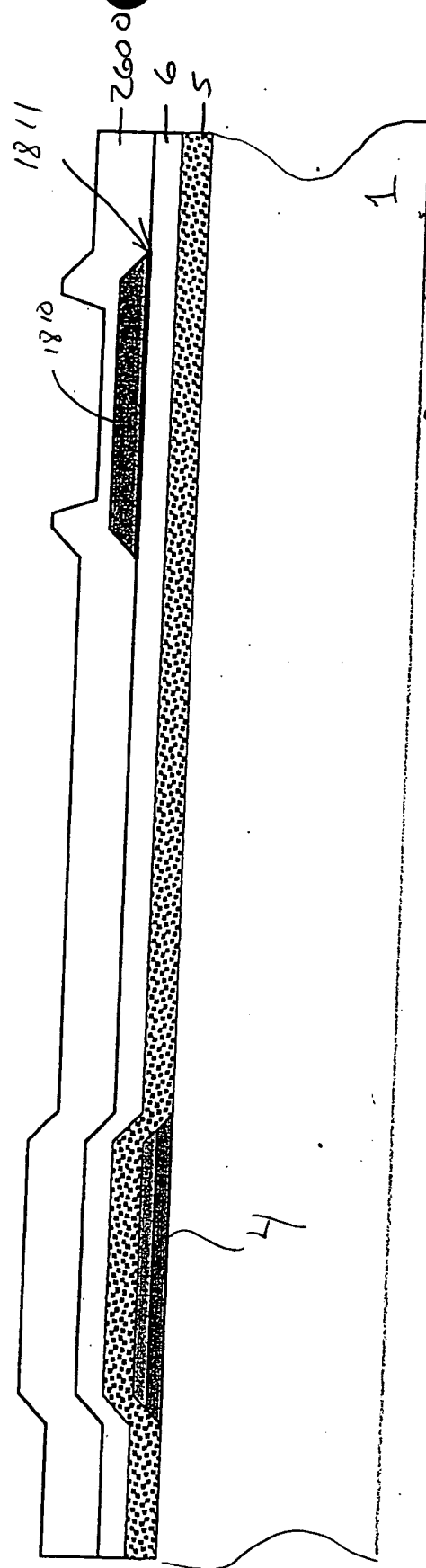
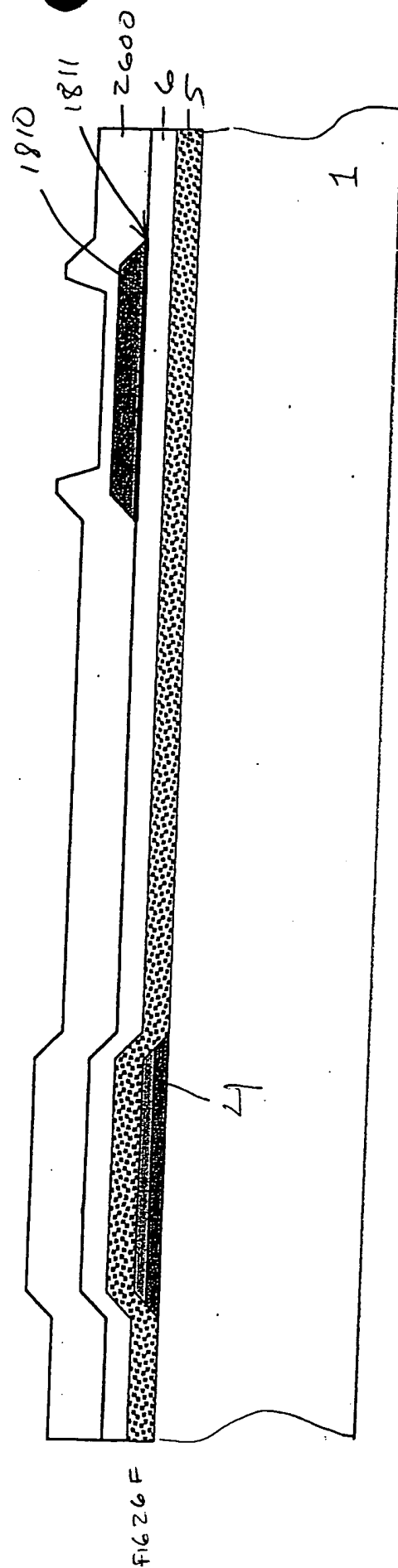
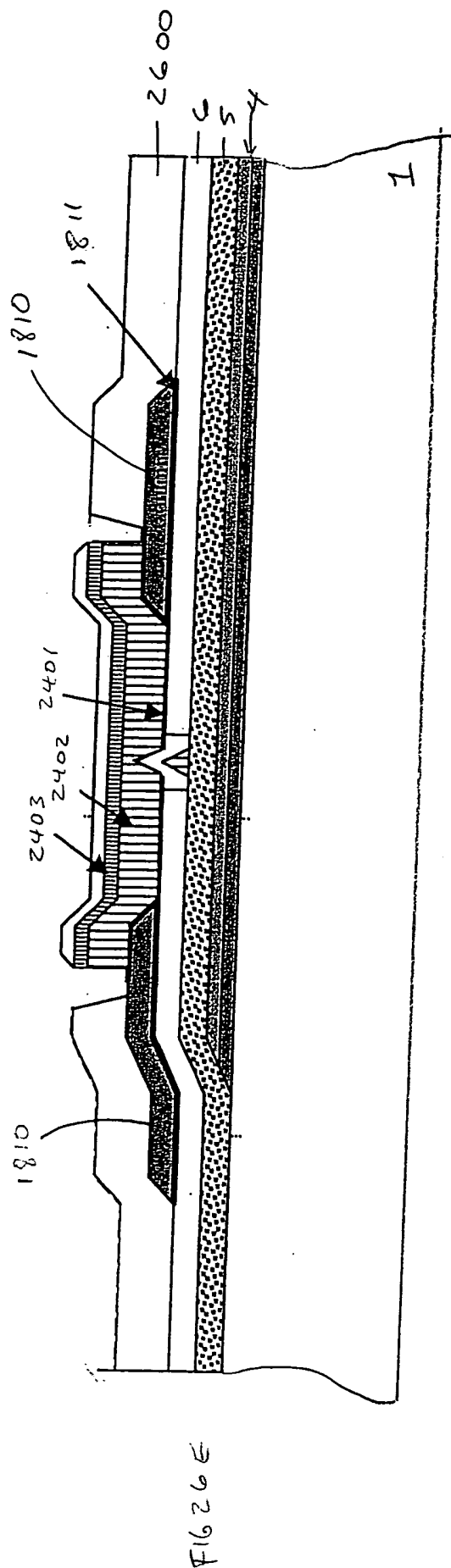


FIG 26D

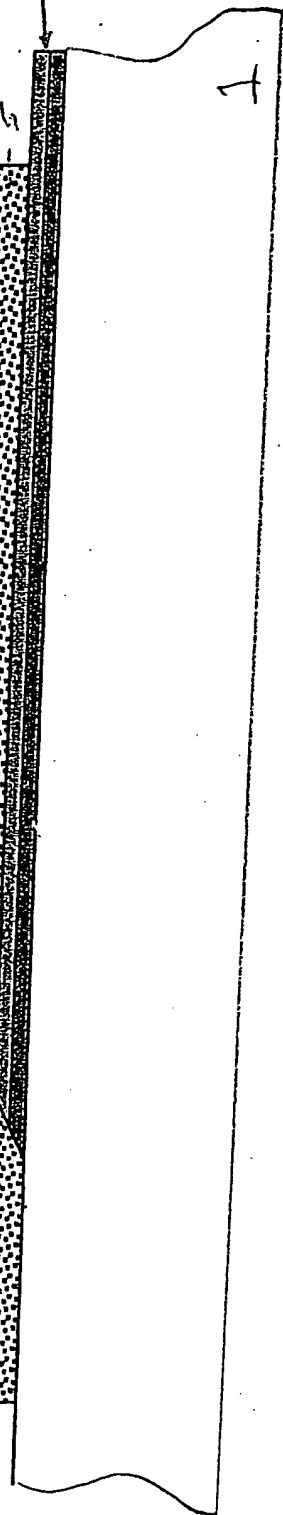


1

1810

2403/2402
2401
1811
1810
2600
6
4

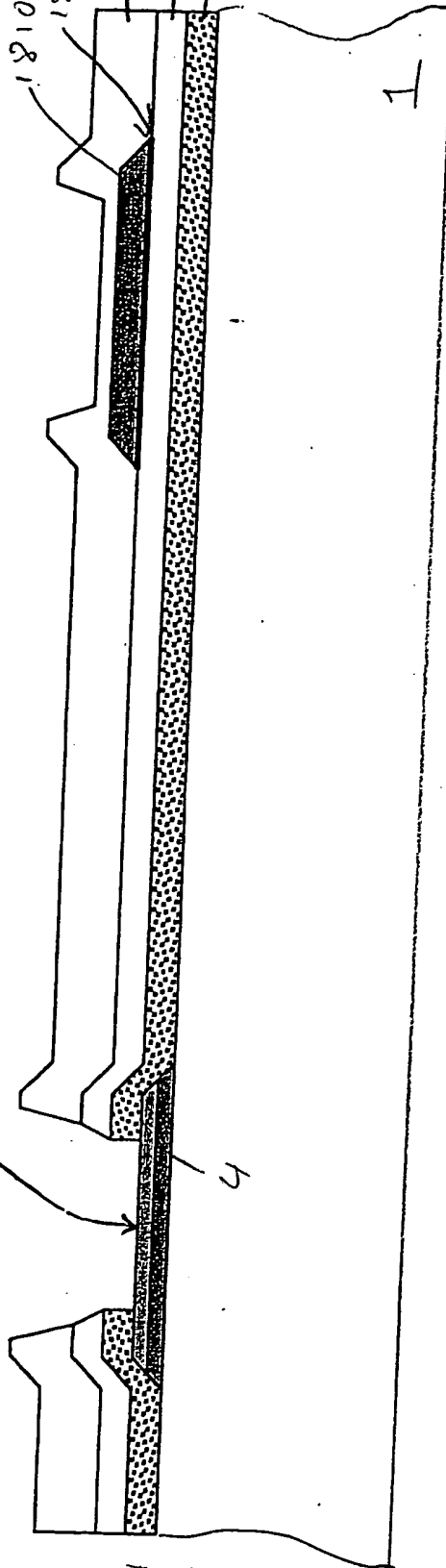
FIG. 26C



2643

1810
1811
2600
6
4

FIG. 26H



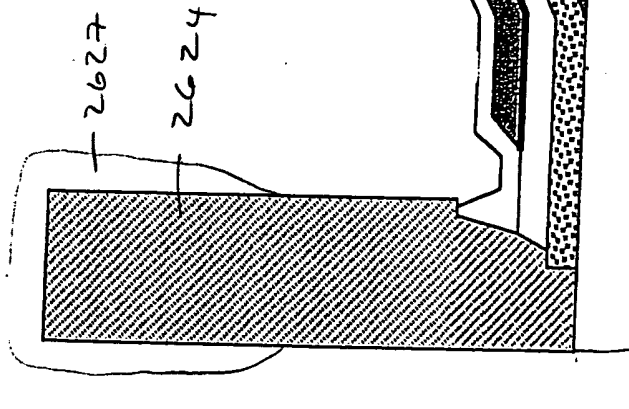


FIG 26K

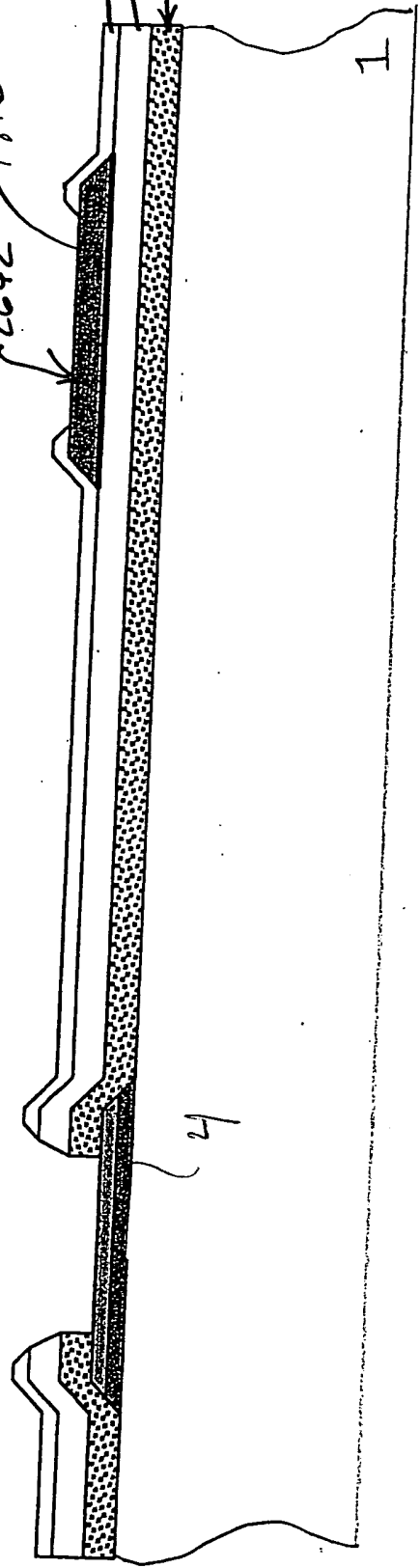
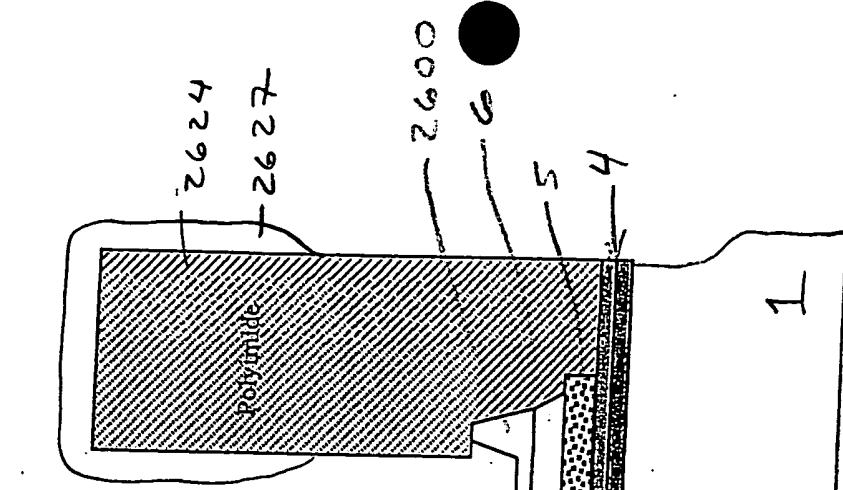


FIG 26L

FIG. 27

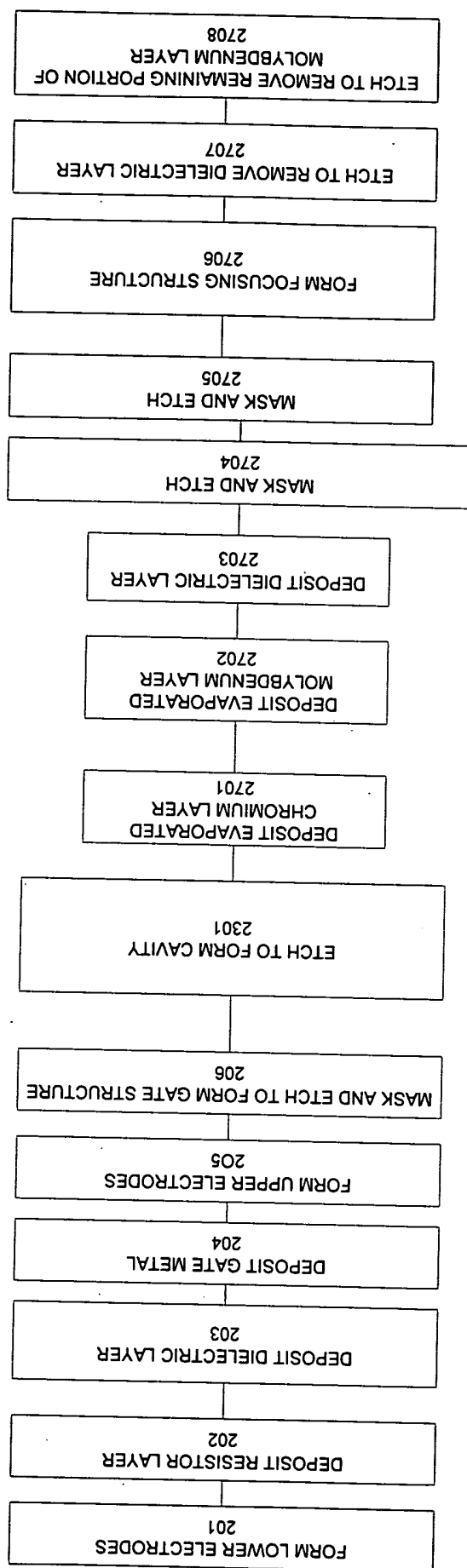


FIG. 27 is a flowchart of a method for forming a semiconductor device. The method includes forming lower electrodes, depositing a resistor layer, depositing a dielectric layer, depositing gate metal, forming upper electrodes, masking and etching to form a gate structure, etching to form a cavity, depositing an evaporated chromium layer, depositing an evaporated molybdenum layer, depositing a dielectric layer, masking and etching, masking and etching, forming a focusing structure, etching to remove a dielectric layer, and etching to remove a remaining portion of a molybdenum layer.

2832

2832
181
2832
2426
2832
181

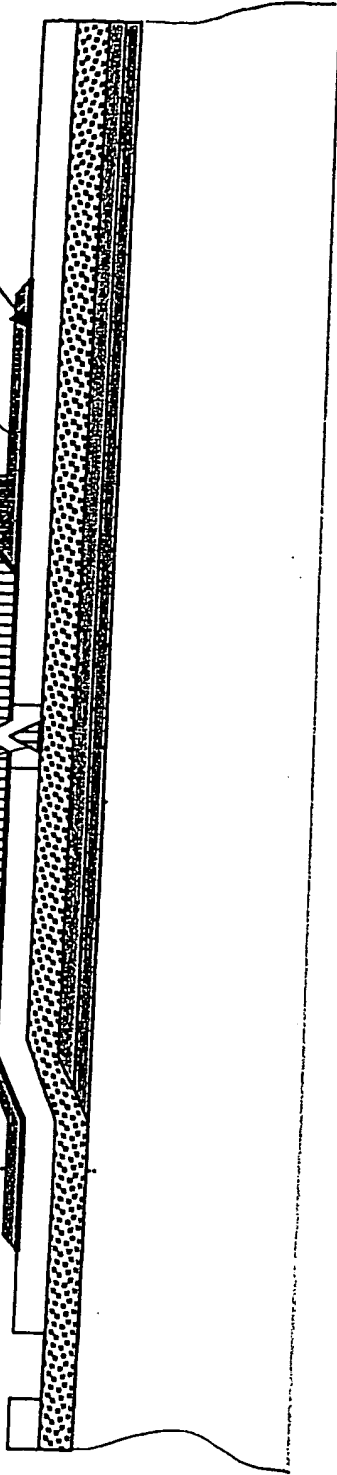


FIG 28C

2832
181
2832
181
2832
181

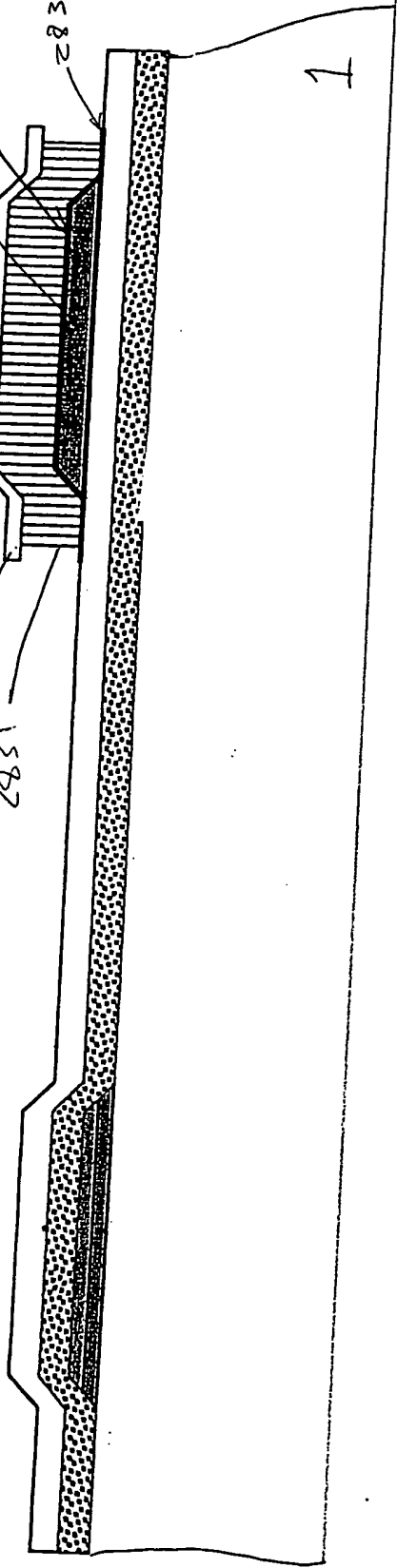
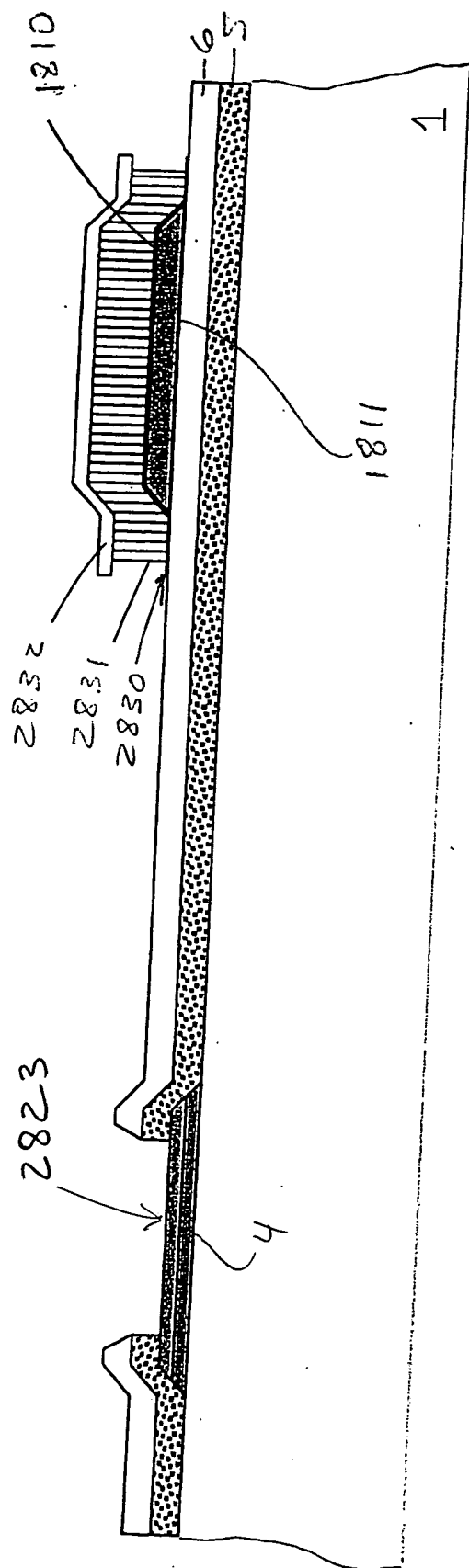
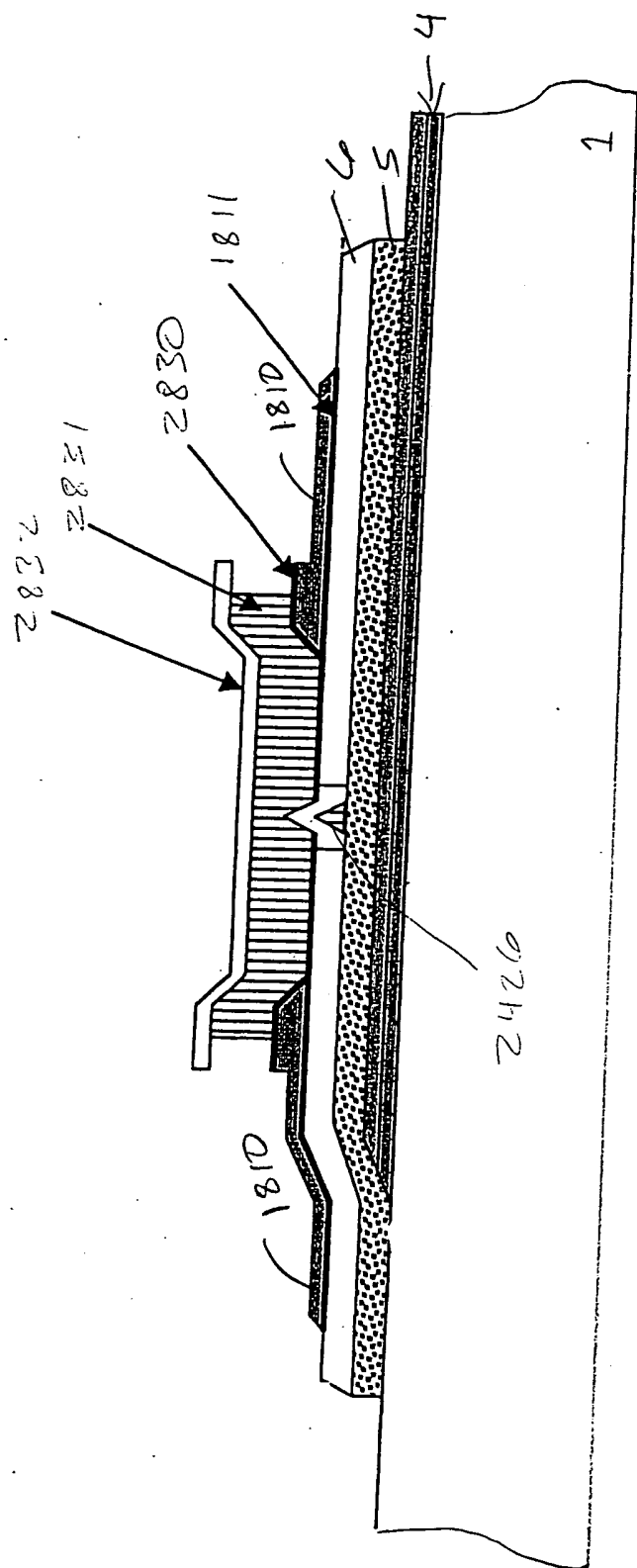


FIG 28D



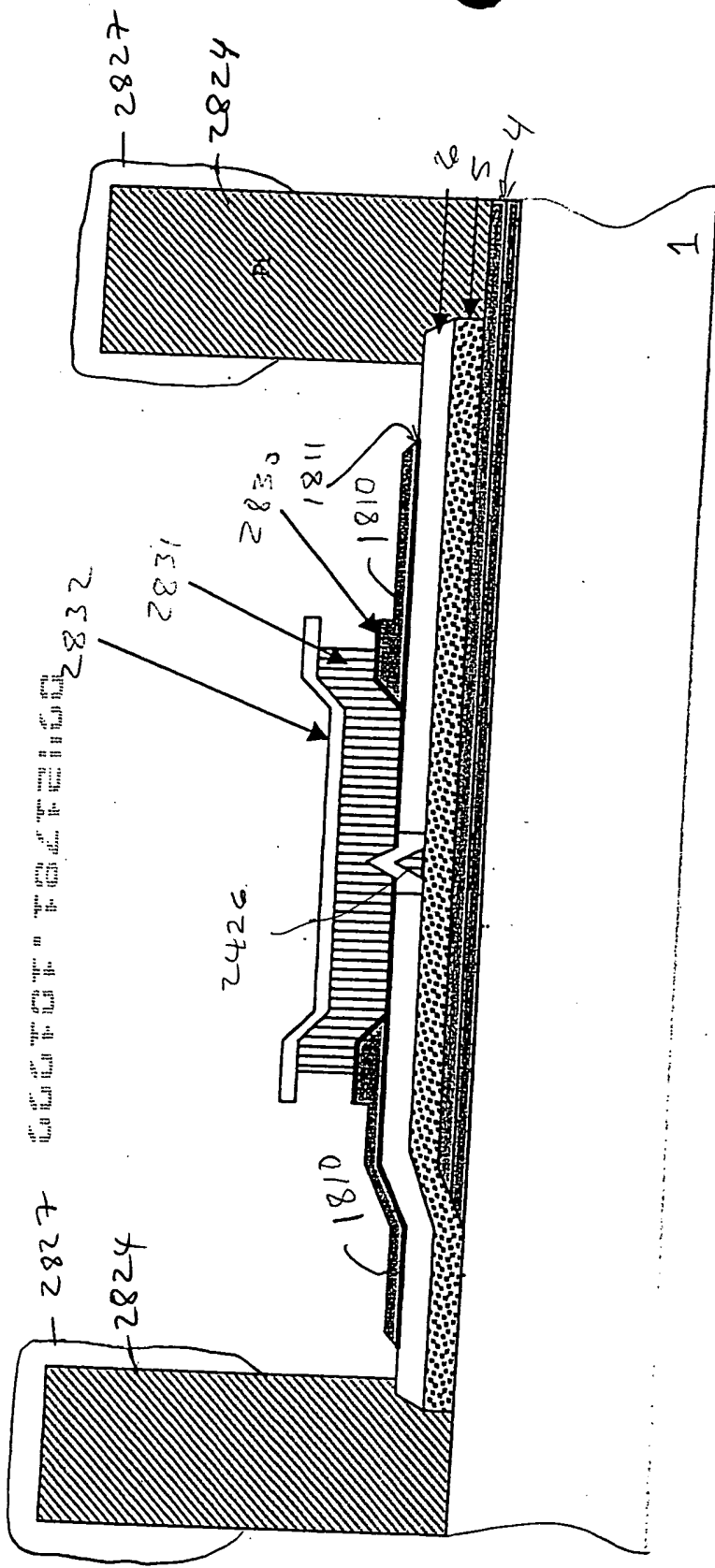


FIG. 28C

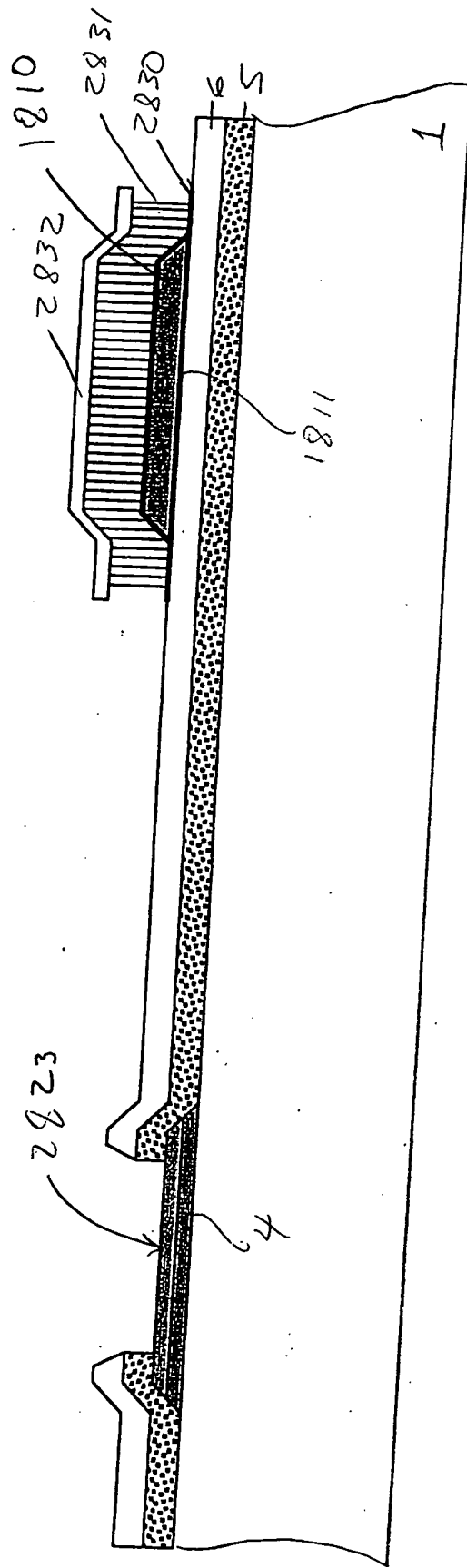


FIG. 28D

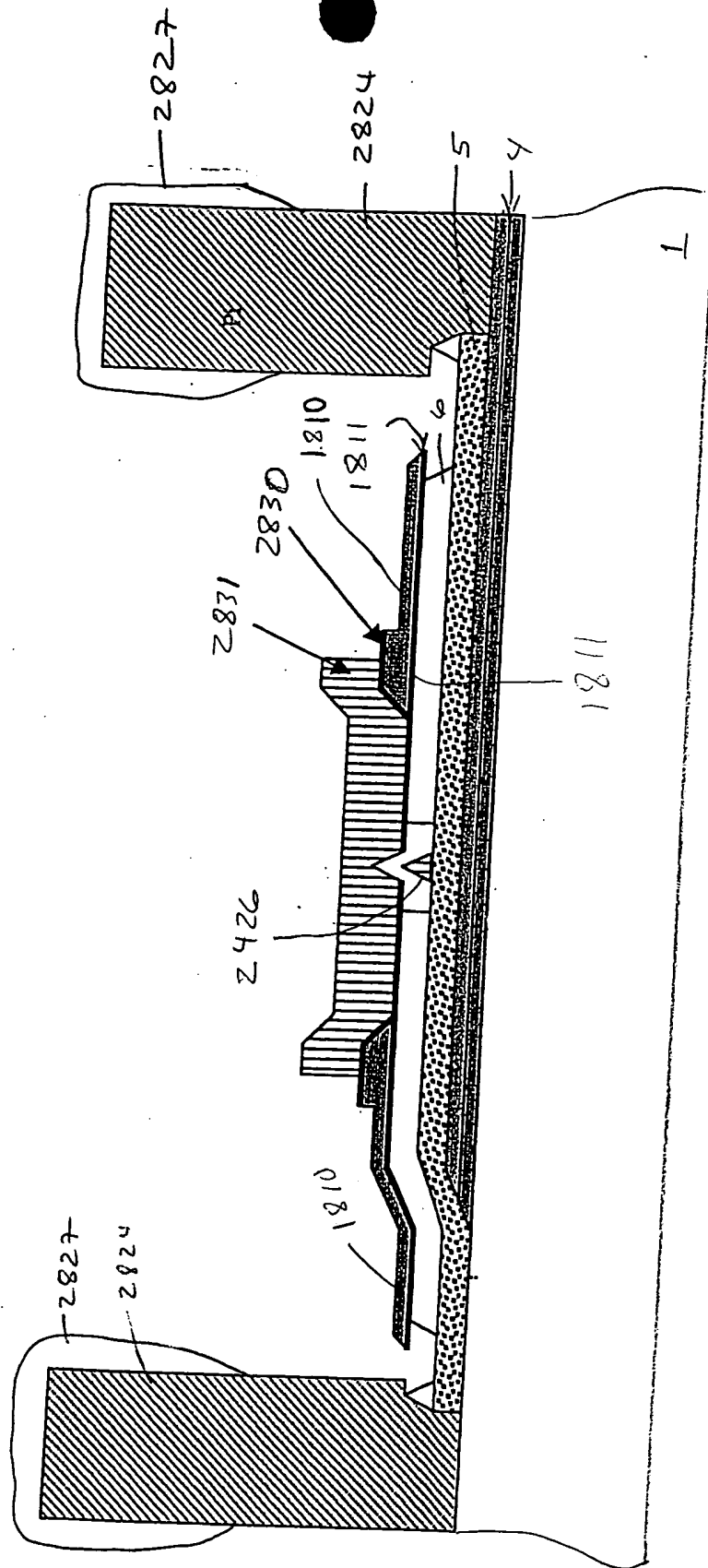


FIG. 282

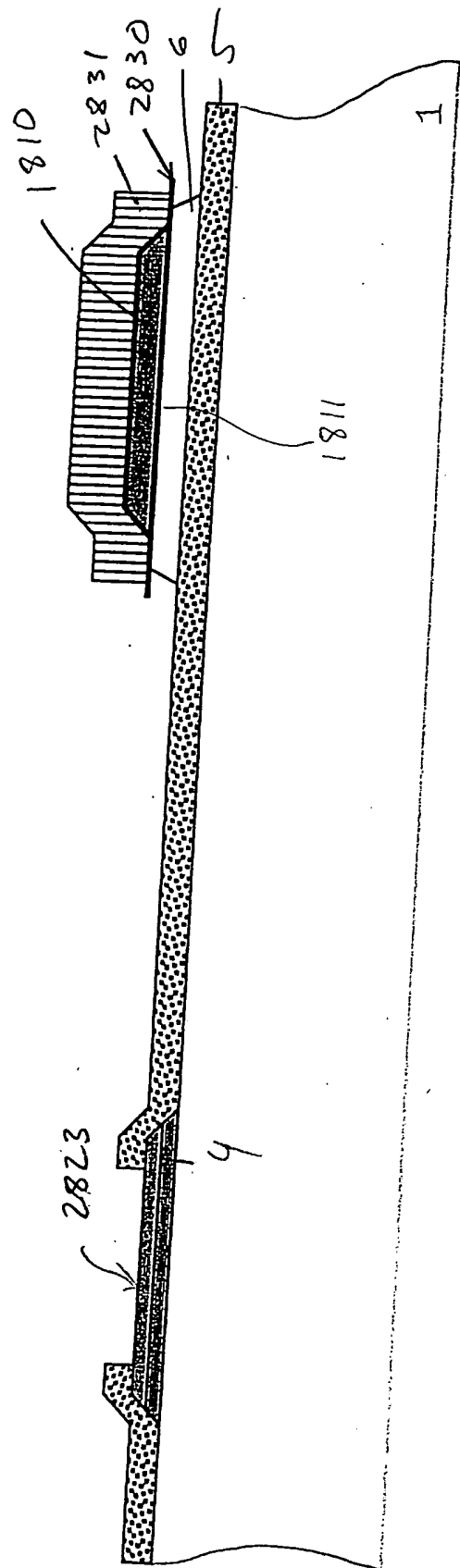


FIG. 283

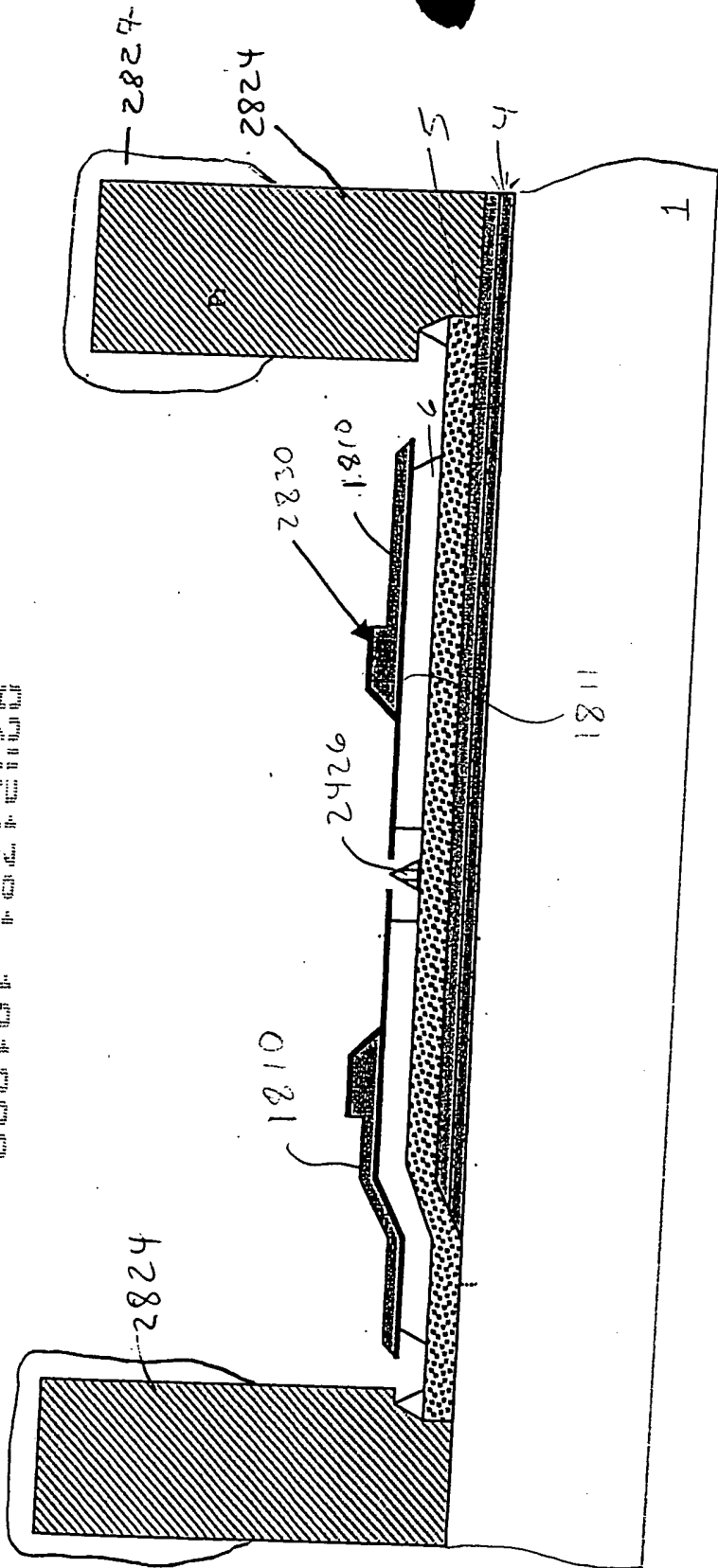


FIG. 28K

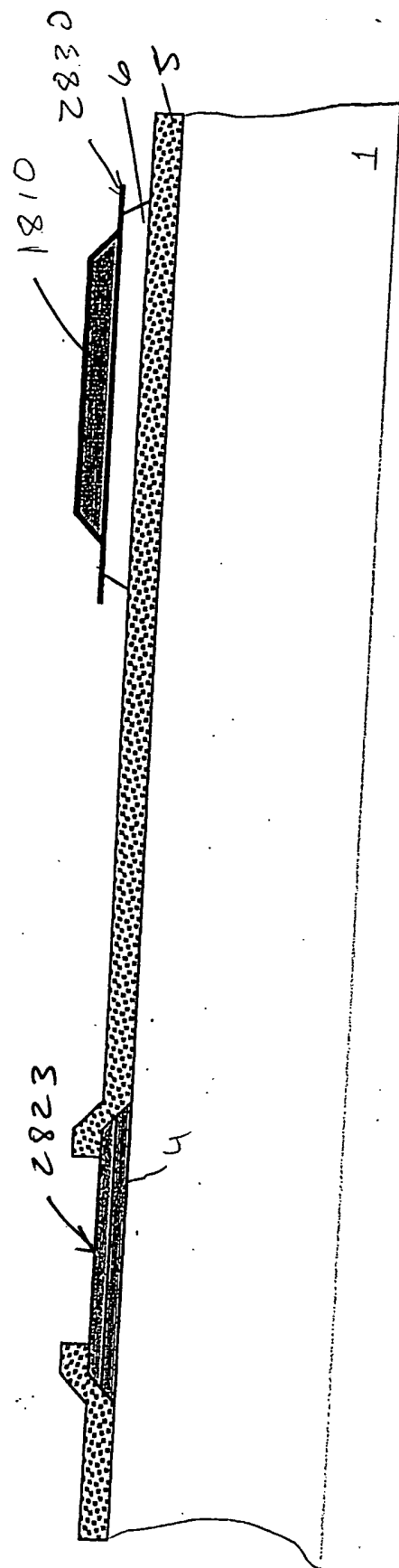


FIG. 28L